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Working document on Specification

HGCROC3

ABSTRACT:
This document is a working document to detail the specification for the HGCROC3.

- Description not differing from the HGCROC2 is in blue.
- New description for HGCROC3 is in black
- Think unclear or in process of change are in red

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HISTORY OF CHANGES

REV. NO.	DATE	PAGES	DESCRIPTIONS OF THE CHANGES
1.0	2019-03-27	n	Data content and Trigger functions added
1.2	2020-13-02	n	-
1.3	2020-03-03	n	-
1.4	2020-03-03	n	-
1.5	2020-03-09	60	Insert relevant information from HGCROCv2 datasheet

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1. 1. HGCROC3: architectural overview

The general block diagram for HGCROC3 is shown in Figure 1.

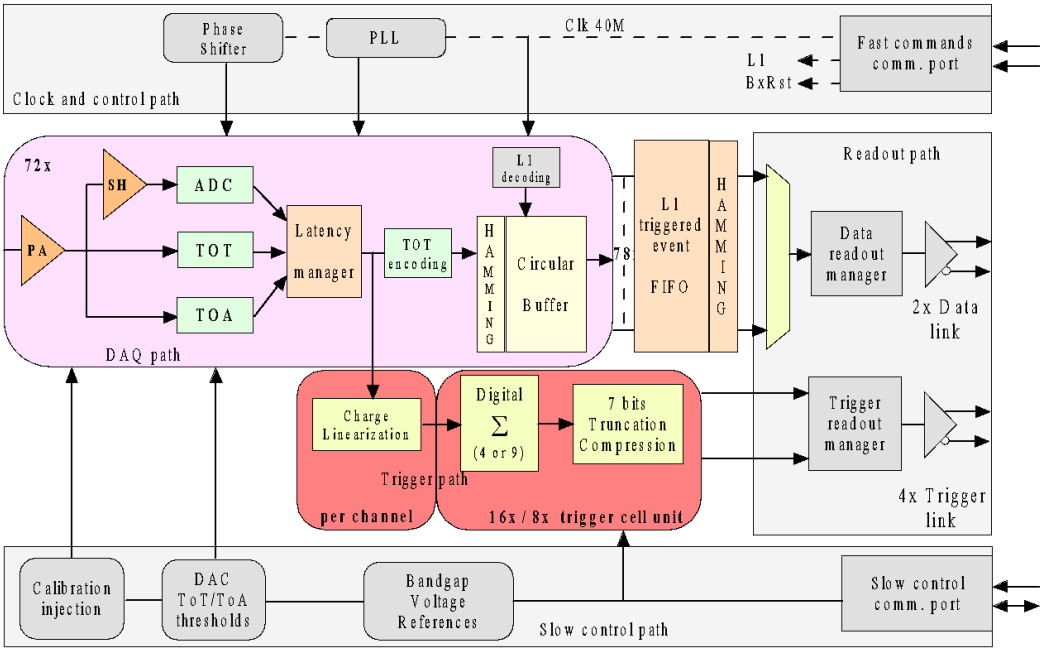


Figure 1: The block diagram for the HGCROC3 ASIC

Most of the blocks and functionality of V2 remains unchanged for V3. The main changes are regarding the digital processing of the DAQ path like the L1 triggered event FIFO, the hamming coding and encoding. For simplicity, the Circular Buffer in the figure above will be called RAM1 and the L1 triggered event FIFO will be called RAM2. Every Control and Command's Modules will be triplicated with TMRG tool. Data encoded inside RAM1 and RAM2 with Hamming. The chip handles 72 channels + 4 channels for common mode subtraction + 2 special calibration channels.

The figure below shows how the charge measurement is provided: in the preamplifier's linear region, the charge is given by the ADC, typically up to 100 MIP. When the preamplifier saturates, the Time-Over-Threshold (TOT) is used to give the charge. The figure below shows how ADC and TOT data combine to give the charge information.

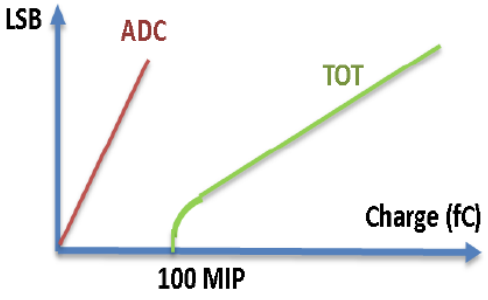


Figure 2: Graphical representation of the individual ADC and TOT charge components.

As the LSB are not equal for “ADC range” and “TOT range”, a linearization step is needed in the trigger path: in the non-linear region of the TOT, a plateau value is applied as shown in the figure below.

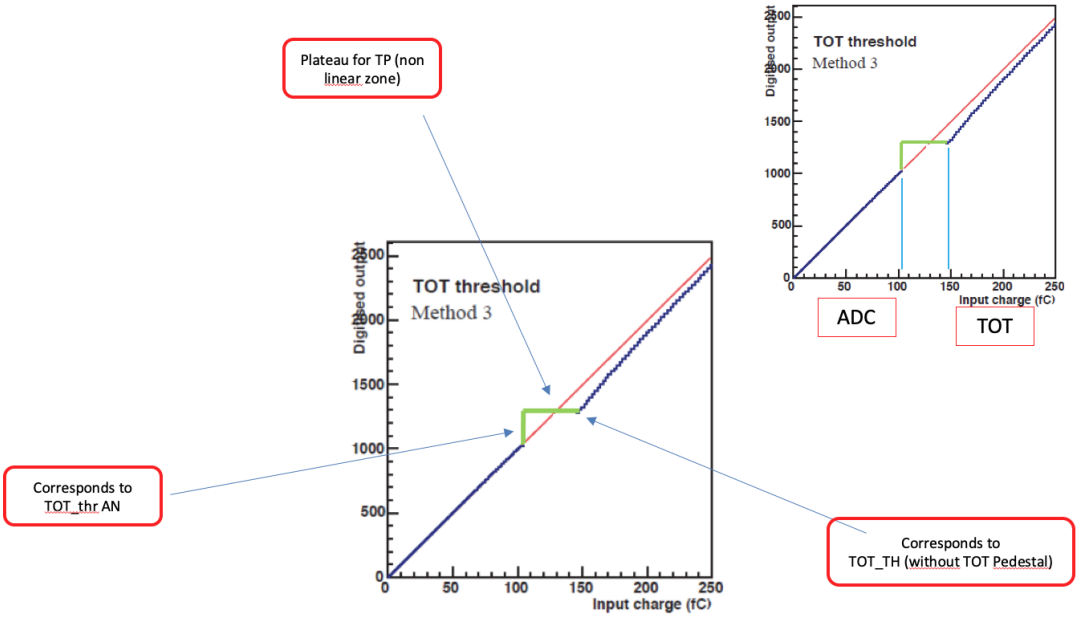
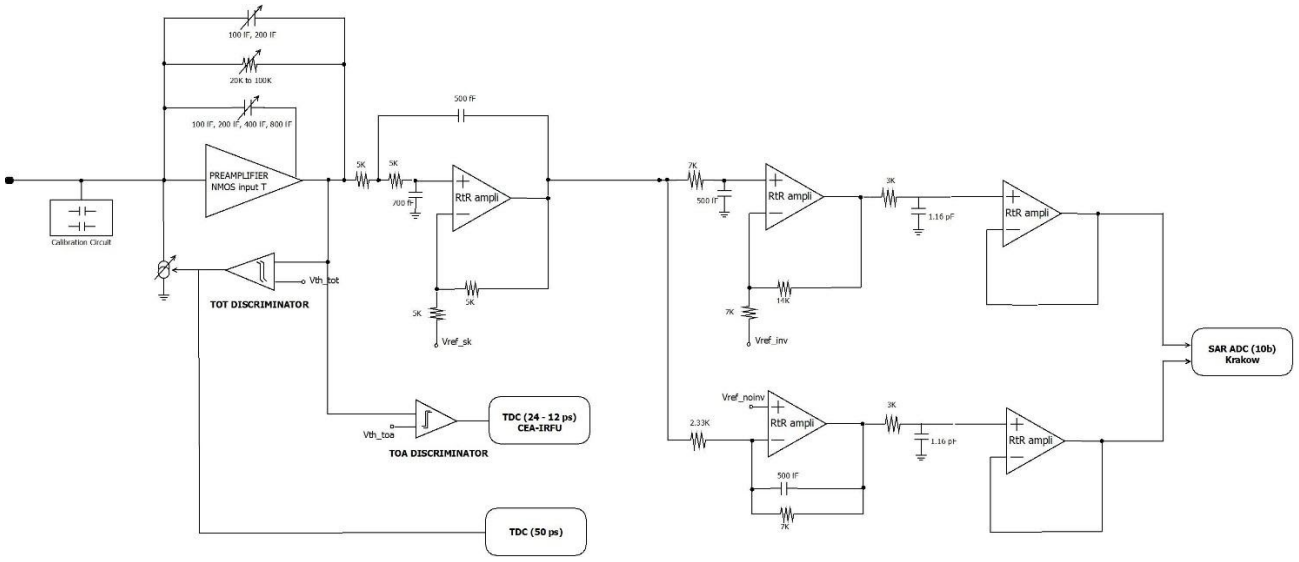


Figure 3: Graphical representation of how the ADC and TOT charge components combine in the TP.

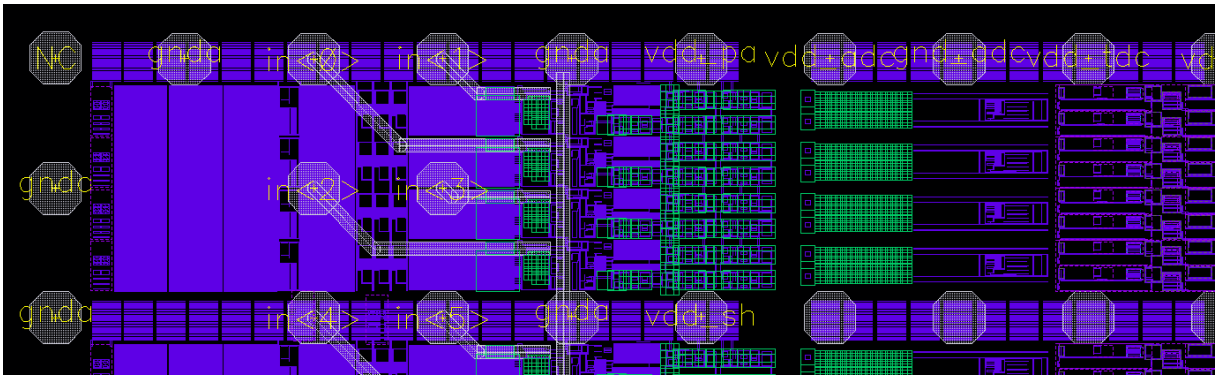
1.1. Analog front-end

The front-end may be divided in three main sub-parts:

- The preamplifier which converts the input charge coming from the silicon diode to an output voltage. It must provide the first amplification of the signal with the best noise performance. In the linear part of the amplifier, the feedback capacitors and feedback resistors provide the gain and the shape of the output signal which is send to the shaper. From the saturation and above, the feedback discriminator triggers and provides the charge measurement by using the “Time Over Threshold” technique (TOT). Another discriminator allows to give the timing information. The preamplifier can be calibrated by injecting a voltage step through two channel-wise selectable capacitors (0.5pF and 8pF).
- The shaper part is composed of three stages: a Sallen-Key filter, a RC^2 filter and a unity gain amplifier to drive the ADC. The shaping time can be adjusted over +/- 20% to compensate for process variations and ensure out of time pileup below 20%.
- The two discriminators providing the TOT and TOA (Time of Arrival) pulses, each one sent to a dedicated TDC.



In order to accommodate the C4 bump bonding pattern, the layout was done in order to fit in 120 µm height and avoid sensitive analog electronics below the bumps. Four channels fit between two rows of pads and the slow control, common to 4 channels, is placed below the pads.



In addition to the 72 readout channels, there are 4 channels for common mode subtraction and 2 channels for MIP calibration. The common mode channels are similar to the regular channels except they stop at the ADC (there are not TDCs). They do not enter the trigger path but are read out in the data path.

In the following sections, more details are given for each block.

1.1.1 1.1.1. Preamplifier

The preamplifier is DC coupled to the input and provides three outputs:

- Outpa connected to the **shaper** and the **TOT discriminator**. Its DC operating point is the same than the preamplifier input (160 - 200 mV).
- outCf_pa connected by default to the **TOA discriminator**. Its DC operating point is around outpa + Vgs (~ 500 mV).

A 8b-DAC is connected to the preamplifier input to absorb the leakage current coming from the sensor. More on this below.

The purpose of the preamplifier is to convert the input charge to a voltage output with the best signal-to-noise ratio and a gain adapted to the MIP signal. It must also provide a “short” signal duration to

mitigate the Out-of-Time pileup effect at the shaper output. To meet all these requirements, the gain and the time constant must be adjustable **(these parameters are global, not channel-wise)**. In the table below, all the possibilities are described:

Rf (Ω)	25K, 50K, 66.66K, 100K	In parallel, these resistors provide 15 values to be adjusted with the Cf and Cf_comp values to get a decay time constant around 10 ns.
Cf (fF)	50, 100, 200, 400	Combined with the Cf_comp capacitors, provide the gain of the preamplifier.
Cf_comp (fF)	100, 200	Same purpose than Cf capacitors, but connected differently to improve the preamplifier stability. From gain point-of-view can be considered in parallel with Cf capacitors.

The following plot shows the preamplifier response to a 10 fC input charge for different choice of gain. The feedback resistor is adjusted so that the Rf*Cf product is constant and so the "duration" of the signal. As can be seen in Fig. 4, an undershoot appears for the highest preamp gain.

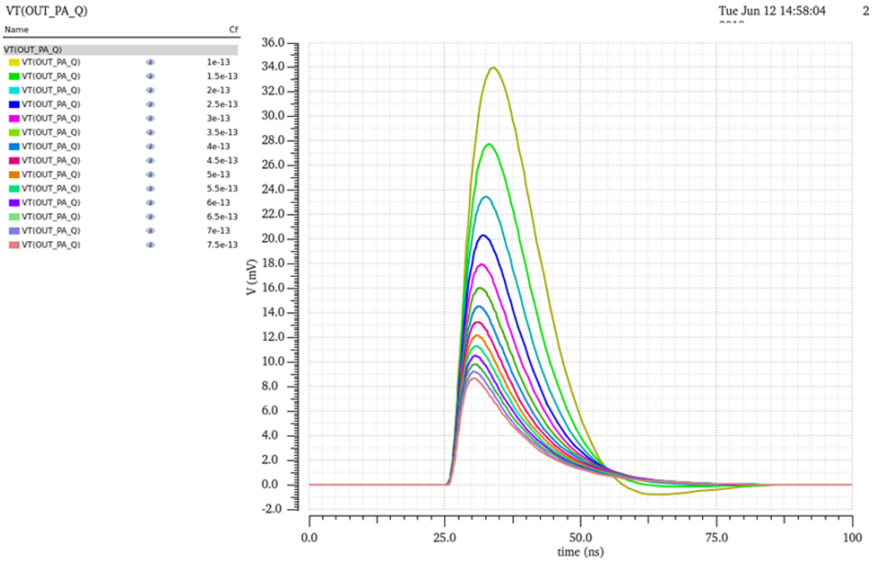


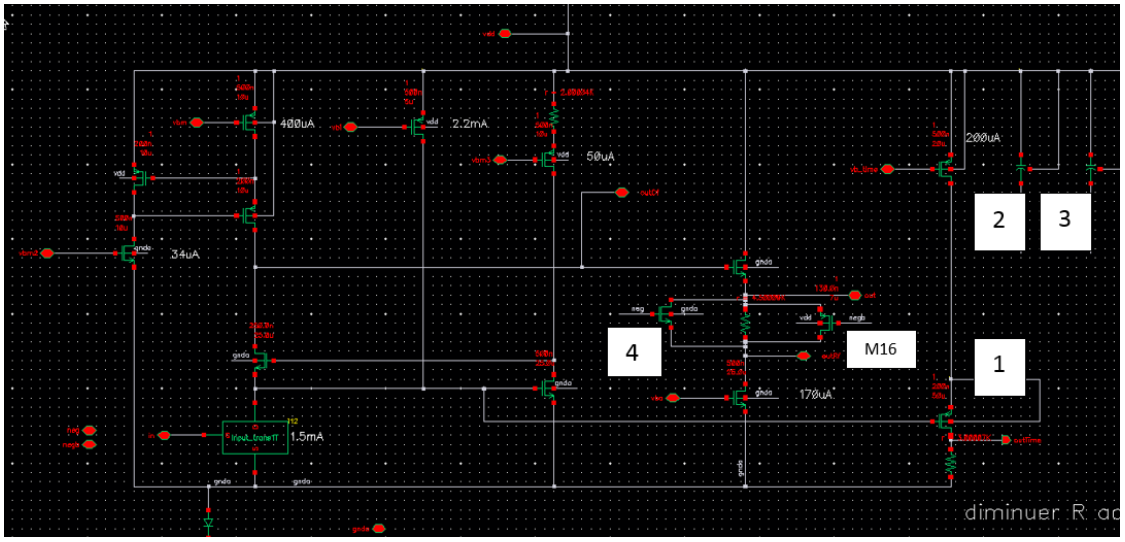
Figure 4 Preamplifier response to a 10 fC input charge for different choice of gain.

Changes in HGCROC3:

Remove unused timing part to increase the speed and the phase margin

1. Remove the common source transistor and resistor
2. Remove the current source to save 200 uA
3. The decoupling capacitors are used to filter vbi_pa (already in V2)
4. The level shifter for negative pulses is kept but not used

Minimum transistor size is M16 7/0.13 (negative polarity switch).

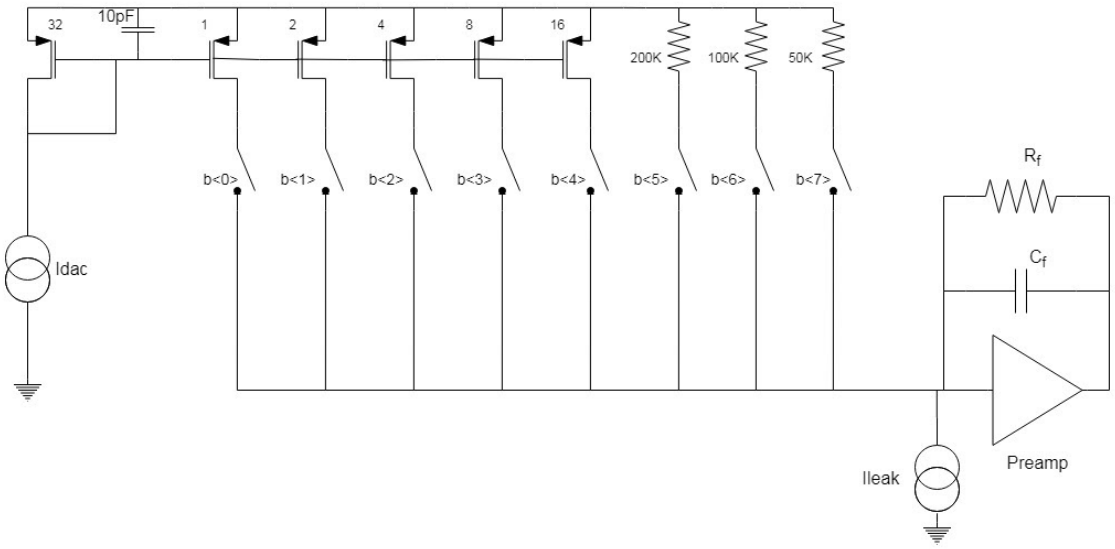


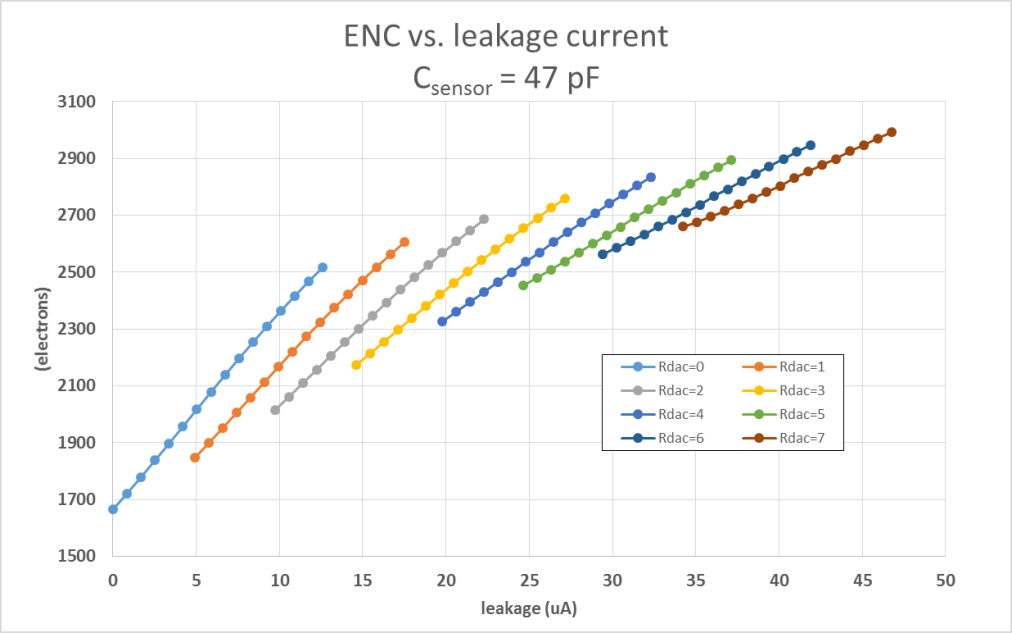
1.1.2. Input DAC (leakage current compensation)

The parallel noise can be reduced by sqrt2 by filtering the current mirror. A 10 pF is taken from vbi_pa to vb_inputdac to filter the noise. The maximum leakage compensation is increased from 10 uA to 50 uA. The DAC is raised from 5 bits to 8 bits by adding a low noise DAC for 5, 10 and 20 uA made with resistors.

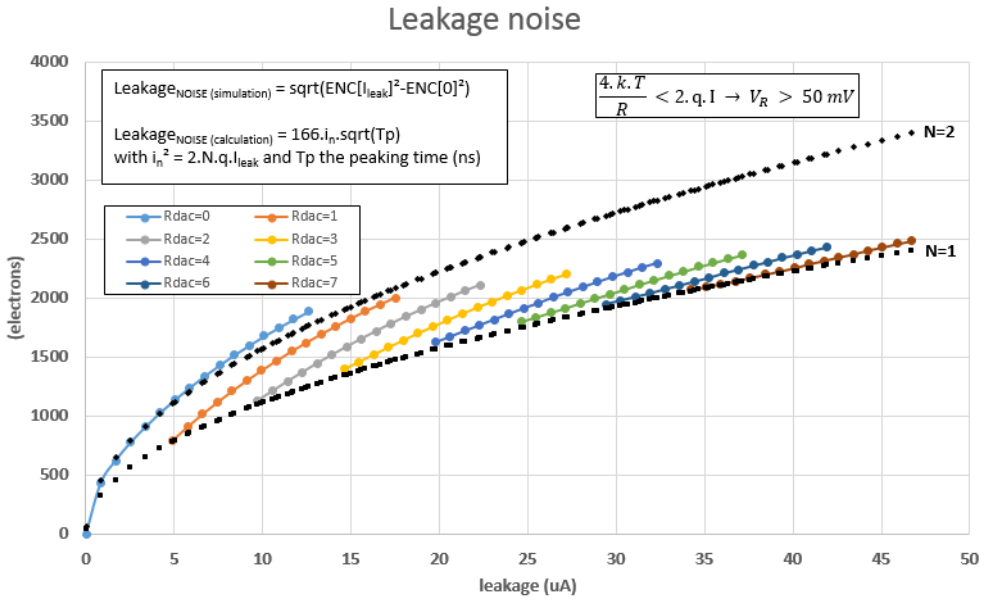
1- Replace all 60/0.13 CMOS switches by 3/0.13 NMOS to reduce leakage
2- Replace 50/0.5um current mirror for leakage current inversion by 5/0.5 to reduce capacitance on input
3- Removes 3/0.15 NMOS cascodes
4- Add 3 bits connected to respectively 50k, 100k and 200k to vdd_dac
5- The dac polarity is now common to all channels

The figure of the new architecture is shown below. The main changes are the 10pF to filter the noise from the master current source, and the 3 resistors to achieve better noise performance at higher leakage current as shown in simulations below.





The figure above shows the total noise (series and parallel) with 47pF sensor capacitance as a function of the leakage current. The figure below shows the leakage noise contribution itself.



The leakage noise in HGCROC-v2 is higher than the blue curve Rdac=0 above: by filtering the input DAC with the 10pF, it follows the N=2 curve. By adding the R-based 3-bits DAC, the leakage noise does not follow the N=2 shape over the full leakage current range but is lowered in-between N=2 and N=1 shapes.

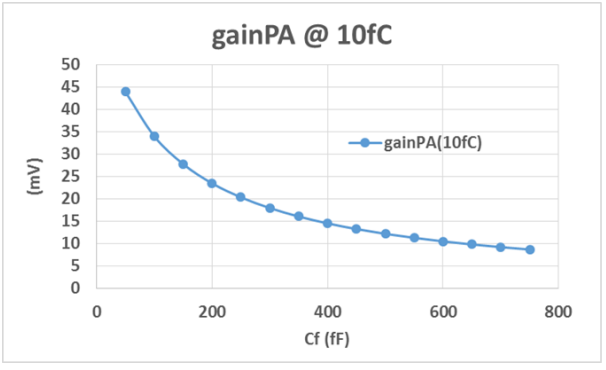
- New measurements are requested: noise w.r.t. the sensor capacitance with all ADC ON, 1 ADC ON, pure analog
- Further simulations: larger resistor to improve the leakage noise performance, in particular around the 5 to 15 uA range.

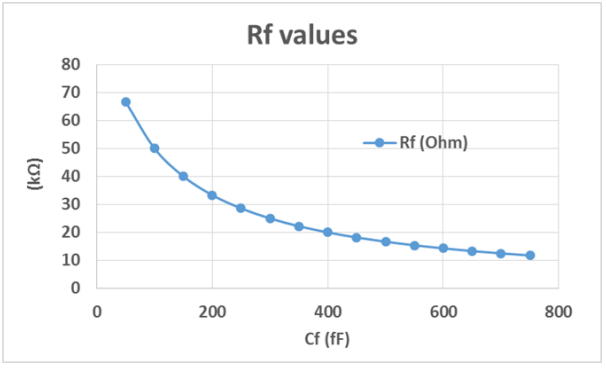
In the table below, all the parameters concerning the preamplifier are described.

Preamplifier parameters

Name	# bits	I2C Sub-block / sub-address	Description
Inputdacpol	1	Channel-wise	Leakage current Input-DAC polarity
Inputdac<8:0>	5	Channel-wise	Leakage current Input-DAC Value (0 µA default; 50 µA max.)
Probe_pa	1	Channel-wise	Preamplifier output probe
LowRange	1	Channel-wise	0.5pF injection cap
HighRange	1	Channel-wise	8pF injection cap
Channel_off	1	Channel-wise	"1" = preamplifier input tied to ground
Trim_vbi_pa<5:0>	6	Global-analog	6b-DAC for preamp input stage current tuning
Trim_vbo_pa<5:0>	6	Global-analog	6b-DAC for preamp output stage current tuning
ON_pa	1	Global-analog	"1" = enable preamplifier bias
Cf<3:0>	4	Global-analog	Preamp feedback cap. <0> = 50fF, <1> = 100fF, <2> = 200fF, <3> = 400fF In //
Cf_comp<1:0>	2	Global-analog	Preamp feedback comp. cap. <0> = 100fF, <1> = 200fF In //
Rf<3:0>	4	Global-analog	Preamp feedback Res. <3> = 25K, <2> = 50K, <1> = 66.66K, <0> = 100K In //
Neg	1	Global-analog	"1" = negative input polarity (Default)
Calib_dac<11:0>	12	Voltage references	Calibration DAC value
IntCtest	1	Voltage references	Selection of the Calibration DAC
ExtCtest	1	Voltage references	Selection of the external pulse test

The two following plots show respectively the preamp gain as a function of the feedback capacitor (with feedback R adjusted so that R*C is constant) and the nominal feedback resistor value for a given Cf value.





As the MIP value is depending on the sensor thickness and the irradiation, the preamplifier gain must be programmable in order to adjust the ADC range to 100 MIPs. The table below summarises the gain specifications.

thickness	MIP		Noise		LSB	ADC range	ADC range	MIP	Noise
	e-	fC	e-	fC	fC	fC	MIP	ch above ped	LSB
120um	9000	1,4	2000	0,3	0,4	320	222	3,6	0,8
120um	**9000**	**1,4**	**2000**	**0,3**	**0,2**	**160**	**111**	**7,2**	**1,6**
120 irrad (worse 3000 fb-1)	**6000**	**1,0**	**2600**	**0,4**	**0,1**	**80**	**83**	**9,6**	**4,2**
200um	15000	2,4	2500	0,4	0,4	320	133	6	1,0
200 um	**15000**	**2,4**	**2500**	**0,4**	**0,4**	**320**	**133**	**6**	**1**
200 irrad (worse)	**6000**	**1,0**	**3000**	**0,5**	**0,1**	**80**	**83**	**9,6**	**4,8**
300 um	**20000**	**3,2**	**2000**	**0,3**	**0,4**	**320**	**100**	**8**	**0,8**
300 irrad (worse 3000fb-1)	**10000**	**1,6**	**2200**	**0,4**	**0,2**	**160**	**100**	**8**	**1,8**
300 irrad (worse 3000 fb-1) high gain	10000	1,6	2200	0,4	0,1	80	50	16	3,5

The table below gives the nominal Cf and Rf values for a given ADC range.

ADC range	Cf	Cf_comp	Rf	Comment
80 fC	200 fF "0100"	0 "00"	50K "0100"	Typical value! Can be more or less adjusted in practice!
160 fC	200 fF "0100"	200 fF "10"	33.33K "0101"	Default slow control values
320 fC	400 fF "1000"	300 fF "11"	16.66K "1100"	Typical value! Can be more or less adjusted in practice!

The preamp gain settings showed above are typical to get the specified ADC range, but since the feedback capacitors can be set from 50 fF to 750 fF and more and the feedback resistor from 11.7K to 100K, there are more possible combinations reaching the specifications. **The Annexe B describes all the combinations of Rf and Cf (TBD, for now cf V2 datasheet).**

Since the preamplifier converts an input charge to an output voltage, its behaviour over the entire charge dynamic must be well known and characterized. That can be divided in three steps:

- The linear mode: the preamplifier provides an output amplitude proportional to the input charge. It is able to provide linear amplitude over ~300mV dynamic range[1] (see red curves in the following plot). The ADC is used to measure the charge in this region which is named ADC range.
- The non-linear mode: this mode occurs in-between the linear and the saturated modes when the preamplifier is no longer linear but not still fully saturated. It is in this region that the TOT threshold has to be set in order to optimize the ADC range linearity. The preamplifier non-linear mode leads to the non-linearity of the TOT in the beginning of the TOT range, but the pile-up limitation is expected to be the best in this region (see violet and blue curves in the following plot and red curves in the next). The non-linear mode occurs for an output amplitude between 500 and 600mV.
- The saturated mode: it occurs for an output amplitude above 600mV (see yellow and greens curves in following plot). In this region, the preamplifier pulse width is proportional to the input charge and so well suited to use the Time-over-Threshold technics. The drawback is the undershoot of the preamplifier signal leading to incorrect charge measurement in the next bunch crossing. The

[1] The linear dynamic range is limited to 300mV because the first stage of the preamplifier is composed of four serial transistors needed to get a large open loop gain (90dB) what implies the first stage output amplitude is limited by a cascode transistor's V_{DS} - V_{DS_SAT} voltage.

193 undershoot is due to the fact that in saturation the preamplifier is in open loop and consequently
194 slower to recover its normal behaviour.

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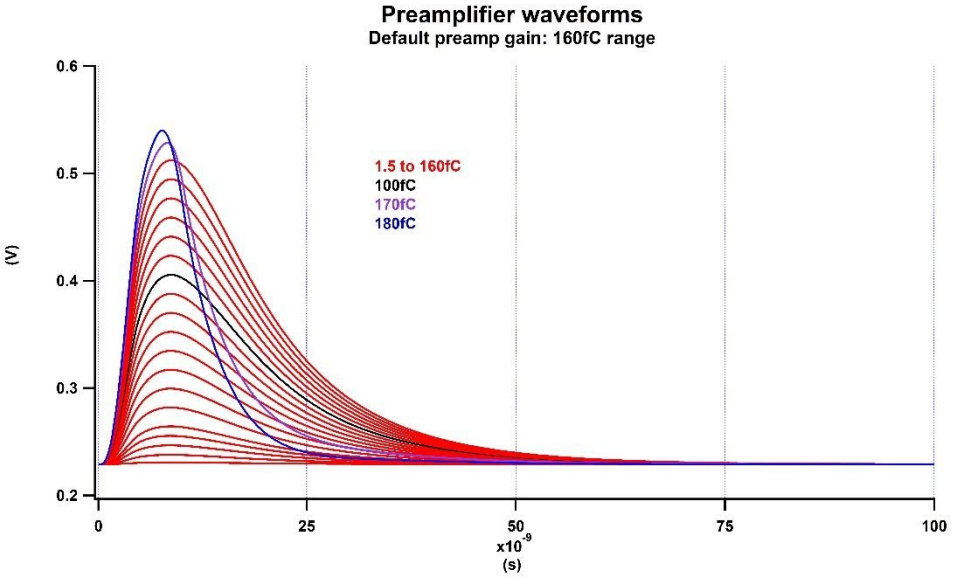

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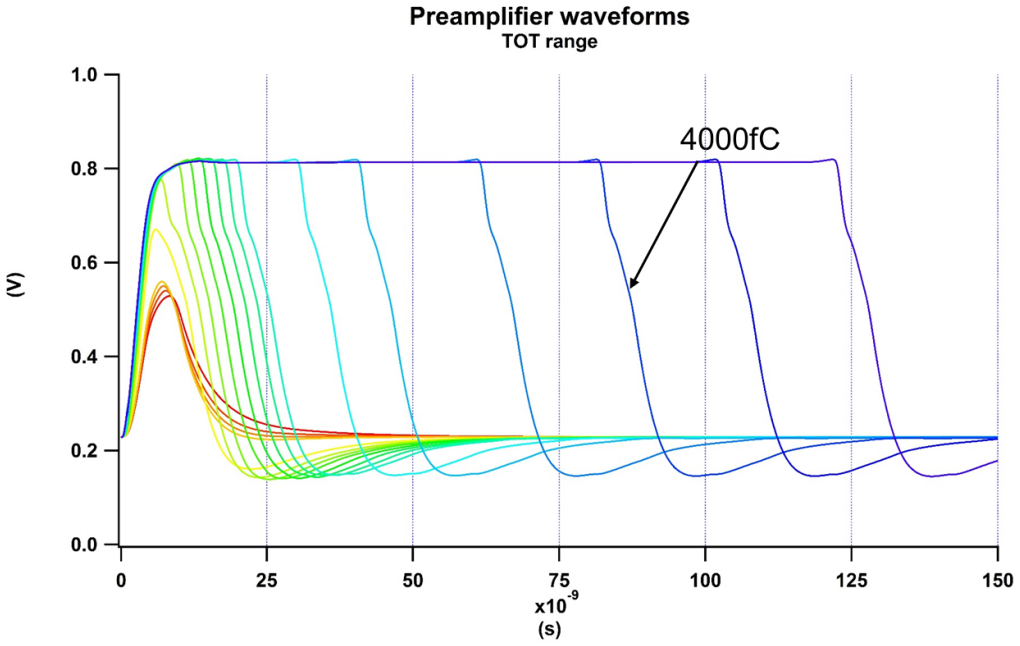

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198 *1.1.1* 1.1.3. Shapers

199 The shaper is divided in three stages:

200 • A Sallen-Key (S-K) shaper, gain 2
201 • A RC^2 shaper, gain 2

- Then a buffer to drive the ADC

It is a 4th order RC shaper with the peaking time typically set around 23ns (shaping time ~ 5ns). The purpose is to optimize the signal-to-noise ratio and use the full available dynamic range (~ 1 V). The signal must be short enough to keep the signal below 20% after 25ns (for the next bunch crossing, to limit the out of time pileup). As the gain and the decay time are given by the preamplifier feedback, the shaper has to ensure the optimal shaping time, between 20 and 25 ns. The shaping time is adjustable over 2 bits to mitigate process variations.

The user has to set the inv_vref and noinv_vref 10b-DACs to globally set the DC levels of respectively the inverter and non_inverter shapers, and so set the ADC pedestal. These 10b-DACs have typically 1mV LSB. In order to reduce the dispersion per channel, the user can play with a channel-wise trimming 5b-DAC: these 5b-DAC have typically 2 mV LSB.

- The inverter shaper output's DC level is equal to 3*(inv_vref<9:0> - trim_dac<4:0>) – 2*V_{inpa}
- The non_inverter shaper output's DC level is equal to 2*V_{inpa} – noinv_vref<9:0>
- With V_{inpa} the preamplifier input's DC level (~ 200 mV).
- The ADC converts the differential voltage (SH_noinv – SH_inv).

1.1.3.1. Optimisation of the « ADC range »

We will introduce a simple circuit to automatically find out the best combination. The principle is to force one of the ADC input to 0.6V, perform a scan of the Vref DAC of the other branch and set it to the value giving the code 256 (266 in fact to have some margin), and then redo the same operation but for the other branch. By construction, this way will optimize the pedestal as well as the dynamic range.

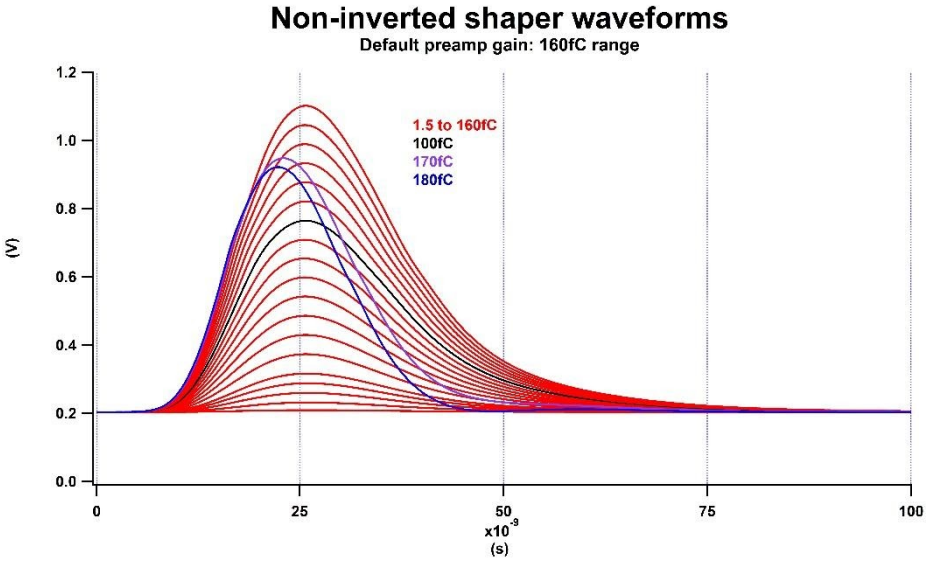
The channel-wise pedestal trimming DAC will be raised from 5b to 6b to better improve the channel-to-channel uniformity.

Shaper parameters

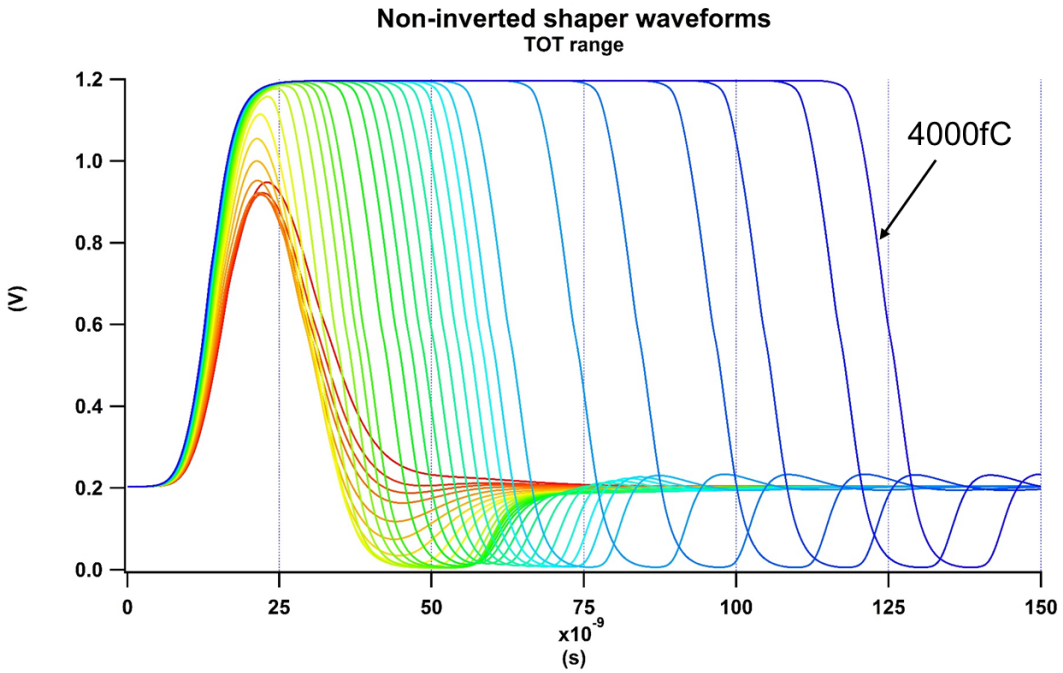
Name	# bits	I2C Sub-block / sub-address	Description
Probe_noinv	1	Channel-wise	Non inverter shaper output probe ("1" = selected)
Probe_inv	1	Channel-wise	Inverter shaper output probe ("1" = selected)
trim_dac_inv<5:0>	6	Channel-wise	Local 6b-TrimDAC for ADC pedestal tuning
ON_rtr	1	Global-analog	"1" = enable shaper amplifiers bias
Ibi_sk<1:0>	2	Global-analog	S-K amplifier input stage current
Ibo_sk<5:0>	6	Global-analog	S-K amplifier output stage current
S_sk<2:0>	3	Global-analog	S-K amp Miller cap. <0> = 50fF, <1> = 100fF, <2> = 200fF
Ibi_inv<1:0>	2	Global-analog	Inverter amplifier input stage current
Ibo_inv<5:0>	6	Global-analog	Inverter amplifier output stage current
S_inv<2:0>	3	Global-analog	Inverter amp Miller cap. <0> = 50fF, <1> = 100fF, <2> = 200fF
Ibi_noinv<1:0>	2	Global-analog	Non Inverter amplifier input stage current
Ibo_noinv<5:0>	6	Global-analog	Non Inverter amplifier output stage current
S_noinv<2:0>	3	Global-analog	Non Inverter amp Miller cap. <0> = 50fF, <1> = 100fF, <2> = 200fF
Ibi_inv_buf<1:0>	2	Global-analog	Inverter buffer input stage current
Ibo_inv_buf<5:0>	6	Global-analog	Inverter buffer output stage current

S_inv_buf<2:0>	3	Global-analog	Inverter buffer Miller cap. <0> = 100fF, <1> = 200fF, <2> = 400fF
Ibi_noinv_buf<1:0>	2	Global-analog	Non Inverter buffer input stage current
Ibo_noinv_buf<5:0>	6	Global-analog	Non Inverter buffer output stage current
S_noinv_buf<2:0>	3	Global-analog	Non Inverter buffer Miller cap. <0> = 100fF, <1> = 200fF, <2> = 400fF
Rc<1:0>	2	Global-analog	Shaping time adjustment
Inv_vref<9:0>	10	Voltage references	Inverter shaper global reference
Noinv_vref<9:0>	10	Voltage references	Non Inverter shaper global reference

The following plot shows the non-inverted shaper output. The red curves correspond to the signal in the ADC range. The violet and blue curves show the response to small "TOT charges". It can be noticed the duration of the signals. Whether it remains 20% of signal in BX+1 in the ADC range (preamplifier linear mode), in the preamplifier non-linear mode, it remains less than 5%.

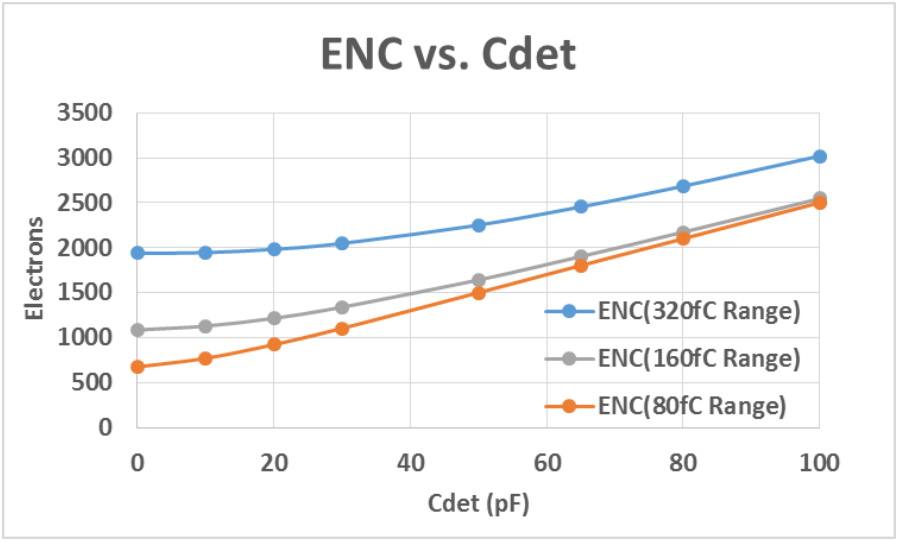


The following plot shows the non-inverted shaper output in TOT range. This TOT range is using the non-linear mode (red curves) and the saturated mode of the preamplifier (yellow and green curves). It can be noticed the undershoot in the saturated region limiting the pile-up efficiency.



The next figure presents the Equivalent Noise Charge (ENC) as a function of the detector capacitance. It may be noticed the lower performance in the low gain mode where the contribution of the parallel noise is more visible.

Clarify: HGCROC 1 or 2?



1.1.4. Discriminators

There are two discriminators per channel, one for the TOT measurement, the other for the TOA.

The TOT discriminator is connected to the outpa output of the preamplifier (160 – 200 mV). The TOA discriminator is connected to the outCf_pa output of the preamplifier (~ 500 mV). Two global 10b-DACs allow the user to adjust the thresholds of the discriminators and two local trimming 5b-DACs allow to reduce the dispersion per channel. The 10b-DAC have typically 1 mV LSB, the trimming 5b-DAC have typically 0.5 mV LSB.

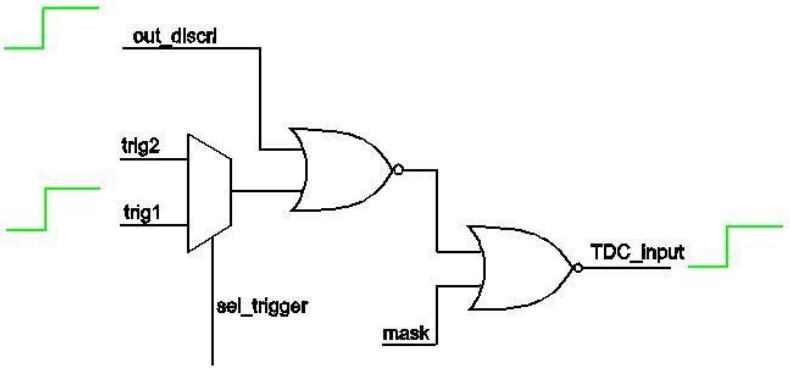
- Toa_Threshold = Toa_vref<9:0> - Trim_dac_toa<4:0>
- Tot_Threshold = Tot_vref<9:0> - Trim_dac_tot<4:0>

There are two external trigger inputs available; typically, in the case when the user wants to calibrate the TOT and TOA, he can send a trigger for the TOA discriminator and the other for the TOT discriminator. He can also send a trigger for a channel, and the other for a neighbouring channel.

The two discriminators outputs can be masked per channel as well.

The following figures shows the principle of the external trigger usage. The Trig1/2 are without effect when they are tied to 0. To send a trigger to a chosen channel, all the others must be masked.

Pull-down resistors are put on the Trig1/2 ports (comparing to V2 where this was not done).



Regarding the TOT discriminator, when it is triggered (output at 0), it enables a constant current source which discharges the preamplifier so that the duration of the preamp signal is proportional to the input charge. This current source can be adjusted over 6 bits in order to adjust the width of the TOT (nominal specification is 200ns for 10 pC).

The two discriminators outputs can be probed and looked at on a scope.

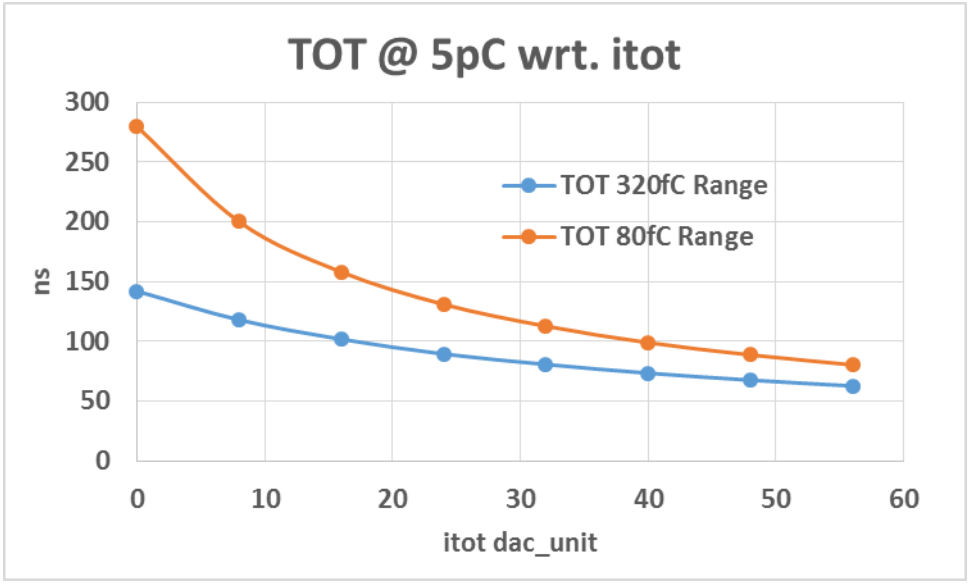
Discriminators parameters

Name	# bits	I2C Sub-block / sub-address	Description
Trim_dac_toa<4:0>	5	Channel-wise	Local 5b-DAC for TOA threshold tuning
Trim_dac_tot<4:0>	5	Channel-wise	Local 5b-DAC for TOT threshold tuning
Mask_toa	1	Channel-wise	TOA discri output mask (“1” = masked)

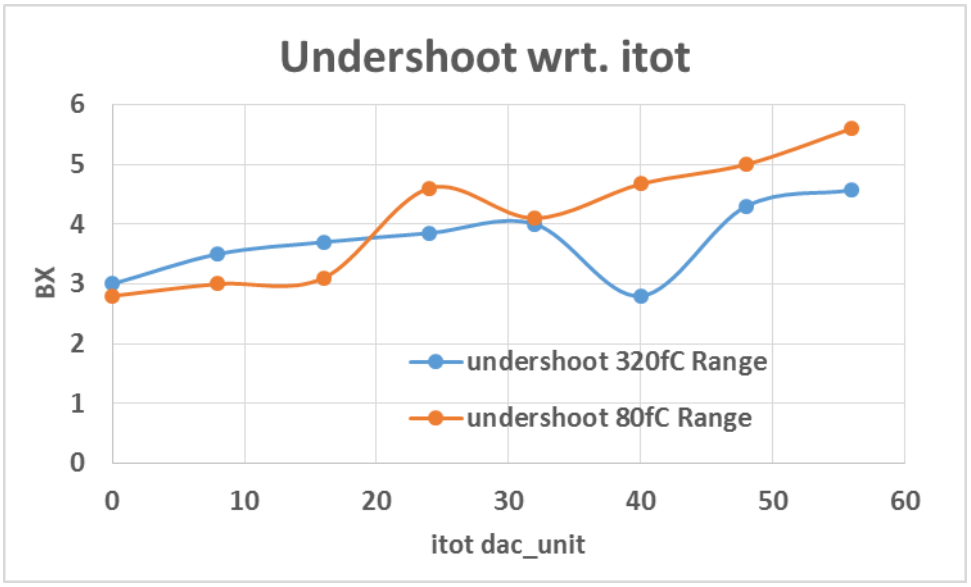
Sel_trigger_toa	1	Channel-wise	External trigger selection for TOA (“0” = Ext Trig1; “1” = Ext Trig2)
Sel_trigger_tot	1	Channel-wise	External trigger selection for TOT (“0” = Ext Trig1; “1” = Ext Trig2)
Mask_tot	1	Channel-wise	TOT discri output mask (“1” = masked)
Probe_tot	1	Channel-wise	TOT discri output probe
Probe_toa	1	Channel-wise	TOA discri output probe
ON_toa	1	Global-analog	“1” = enable TOA discri bias
ON_tot	1	Global-analog	“1” = enable TOT discri bias
Dac_itot<5:0>	6	Global-analog	6b-DAC for TOT gain tuning (“000000” = no feedback current as the original TOT architecture)
En_hyst_tot	1	Global-analog	“1” = enable the TOT discri hysteresis
Pol_trig_toa	1	Global-analog	Polarity of the TOA discri output
Tot_vref<9:0>	10	Voltage references	TOT threshold global value
Toa_vref<9:0>	10	Voltage references	TOA threshold global value

The following figure shows the TOT duration at 5 pC injected charge as a function of the constant current itot. (the specification gives 100ns TOT at 5pC)

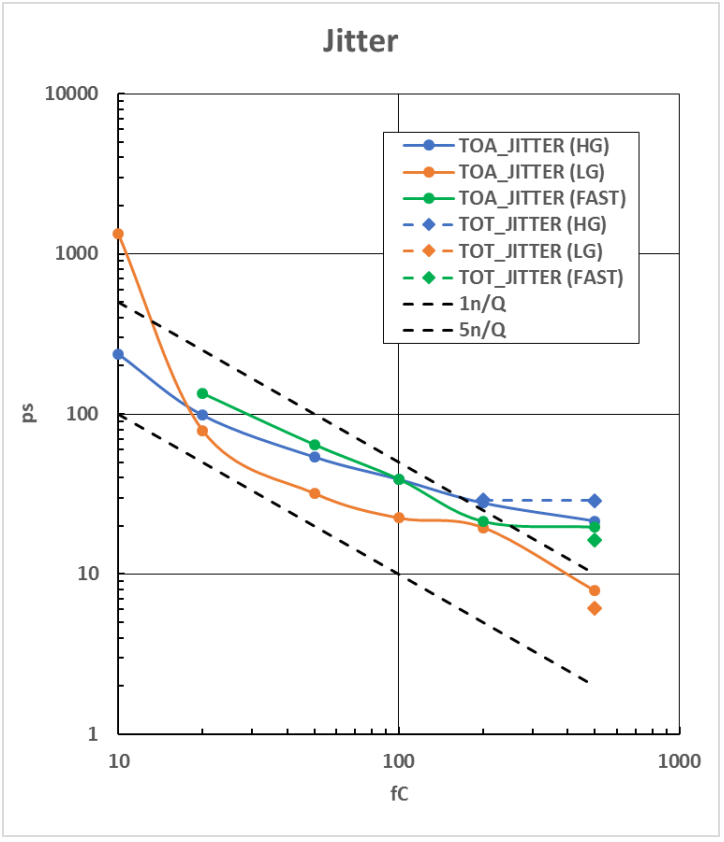
Clarify/update plots for HGCROC3 if needed

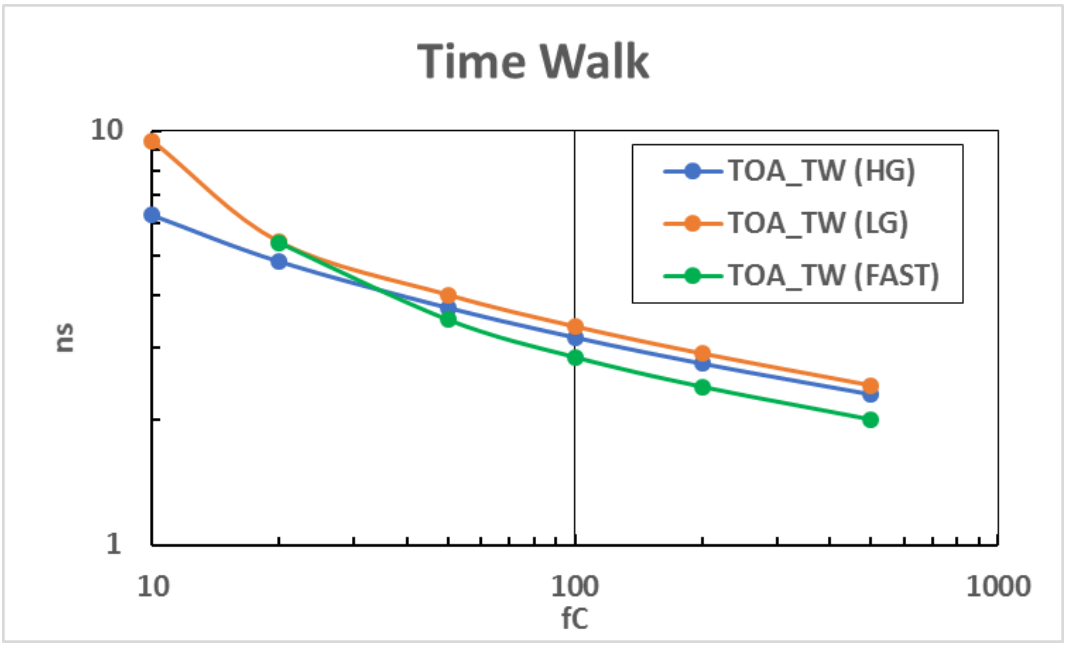


The following figure shows the duration of the “TOT dead time” expressed in Bunch Crossing count, namely the duration from the end of the TOT pulse up to the moment where the ADC gets the pedestal back. (to be noticed that itot=0 corresponds to the very first design)



The two next figures give respectively the jitter and time walk curve as a function of the input charge.

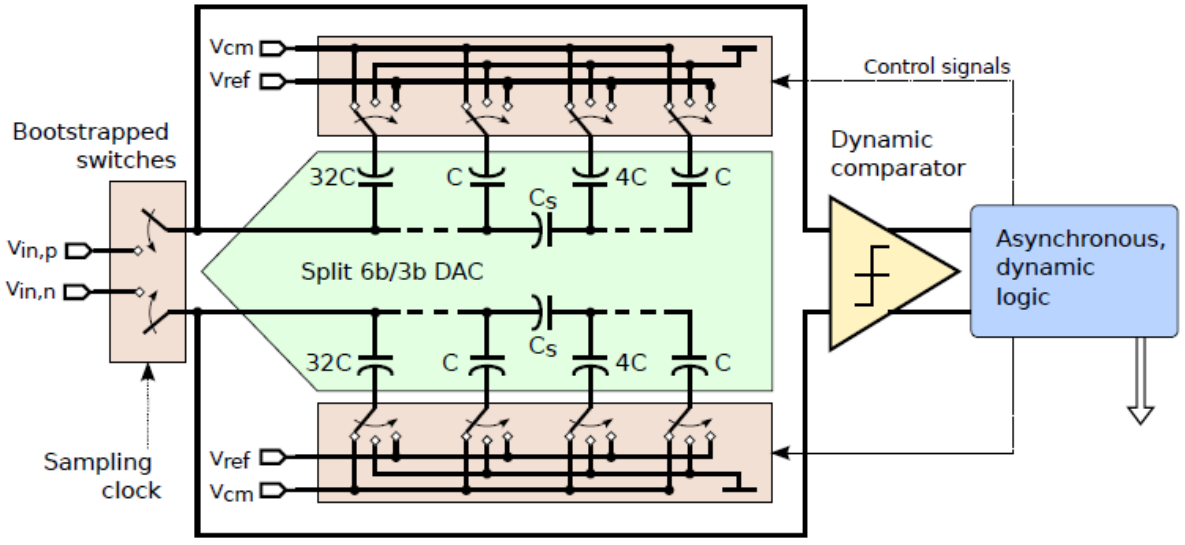




1.2. Mixed-signal blocks

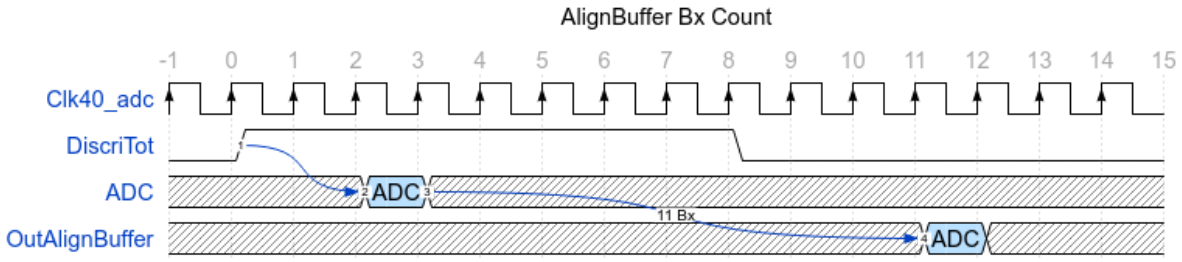
1.2.1. 10bits ADC and Align Buffer

The HGCROC3 contains a 10b SAR ADC, designed by AGH in Krakow. The ADC's vrefm reference voltage is tied to ground.



The 10 bits data provided by the ADC are sent to an Align Buffer to align them to the TOT and TOA data. Indeed, the TDCs providing the TOT measurement introduce a latency due to the duration of the TOT itself (this latency is tuneable in the TDCs). The ADC + Align Buffer have a fixed latency of 11 bunch crossings:

sampling at BC=1, ADC data available at BC=2, data at the Align Buffer outputs at BC=11 (see next chronogram).



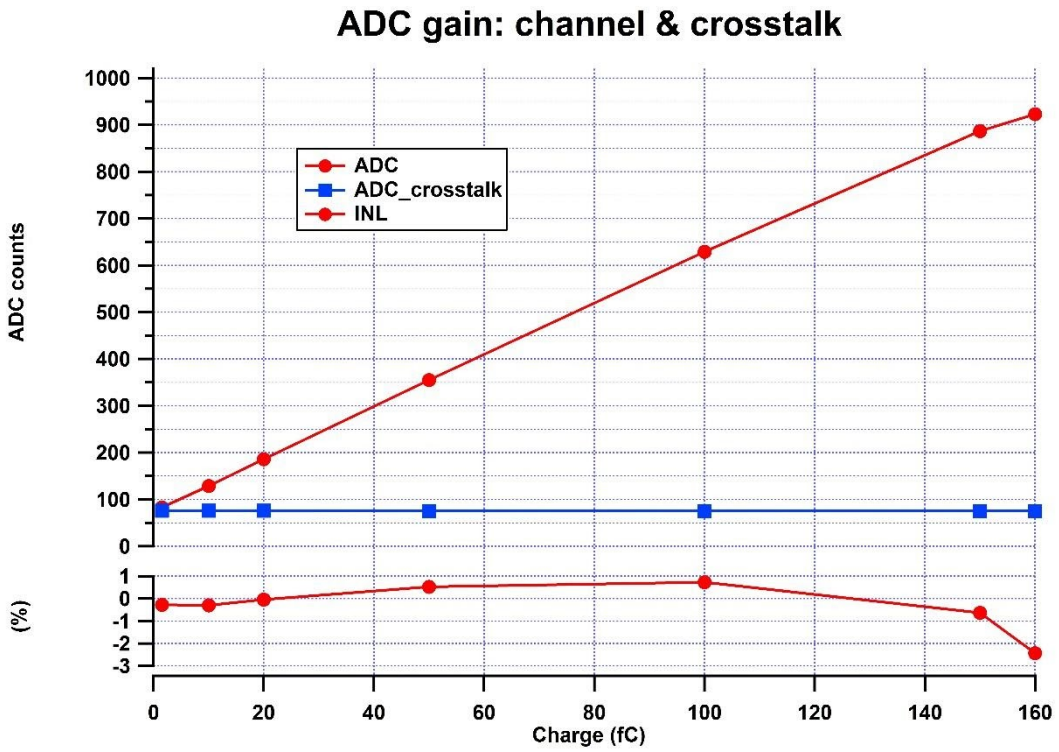
ADC parameters

Name	# bits	I2C Sub-block / sub-address	Description
Mask_adc	1	Channel-wise	"1" = ADC clock off
maskAlignBuffer	1	Channel-wise	"1" = AlignBuffer clock off
Adc_pedestal<7:0>	8	Channel-wise	ADC pedestal value (use in Trigger path)
ExtData<9:0>	10	Channel-wise	Forced ADC data (enable ExtData by SelExtADC parameter: bit 3, register 10, "Global Analog"
Clr_ShaperTail	1	Global-analog	Force ADC to 0 for 2 BXs after the TOT to remove the undershoot
SelRisingEdge	1	Global-analog	"1" = AlignBuffer provides data on rising edge
SelExtADC	1	Global-analog	"1" = Forced ADC data send to the DRAM
Clr_ADC	1	Global-analog	Force ADC to 0 when TOT signal @ 1
Ref_adc<1:0>	2	Global-analog	Input stage current of the Ref ADC OTA
Delay40<2:0>	3	Global-analog	Delay tuning for bits <4:0> "000" = faster conversion
Delay65<2:0>	3	Global-analog	Delay tuning for bits <6:5> "000" = faster conversion
Delay87<2:0>	3	Global-analog	Delay tuning for bits <8:7> "000" = faster conversion
Delay9<2:0>	3	Global-analog	Delay tuning for bit <9> "000" = faster conversion
ON_ref_adc	1	Global-analog	"1" = enable ADC ref OTA
Pol_adc	1	Global-analog	ADC input swap

The user can choose to force ADC data to 0 when the TOT pulse is at 1 (Clr_ADC="1"), otherwise it provides the actual ADC values.

As after a TOT the shaper returns to the pedestal after a given time, the user can also choose to force ADC data to 0 for two next bunch crossing after the end of the TOT pulse (Clr_ShaperTail="1").

The following plot shows the linearity and the INL expressed in % of the ADC range in the default parameters setting.



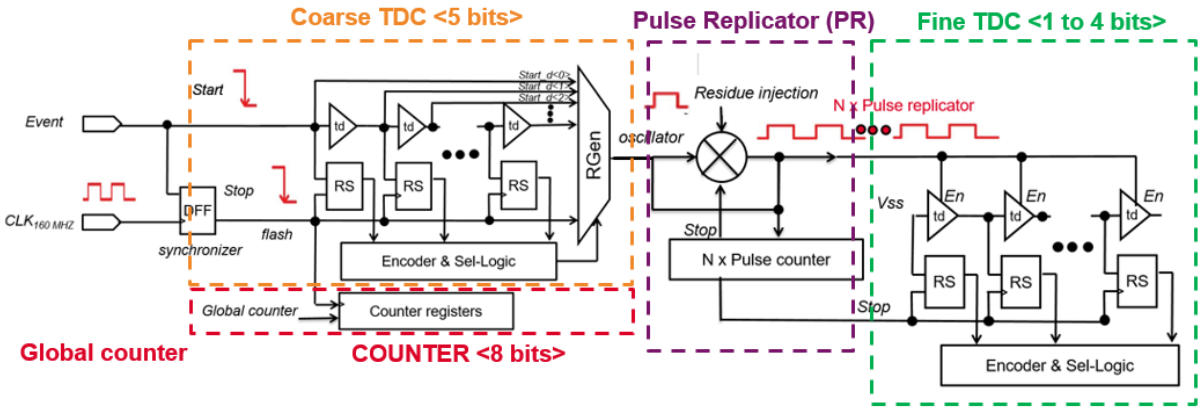
1.2.2. TOT and TOA TDCs

One TDC block handles the TOA and TOT measurements. It was designed by the CEA IRFU group in Saclay. The two following tables give the specifications respectively for the TOA and the TOT.

TDC ToA specifications	
Resolution	about 25 ps RMS
Range	10 bits over 25 ns
Conversion rate	> 40 MHz (bunch clock)
Power consumption	< 2 mW / channel
Area	Pitch 120 µm
Technology	TSMC 130 nm
Temperature	-30 °C

TDC ToT specifications	
Resolution	< 50 ps RMS
Range	12 bits over 2-200 ns
Min time between hits	25 ns
Power consumption	< 2 mW / channel
Fixed latency	12 clock periods
Technology	TSMC 130 nm
Area	Pitch 120 µm
Temperature	-30 °C

The schematic below gives an overview of the TDC circuitry.

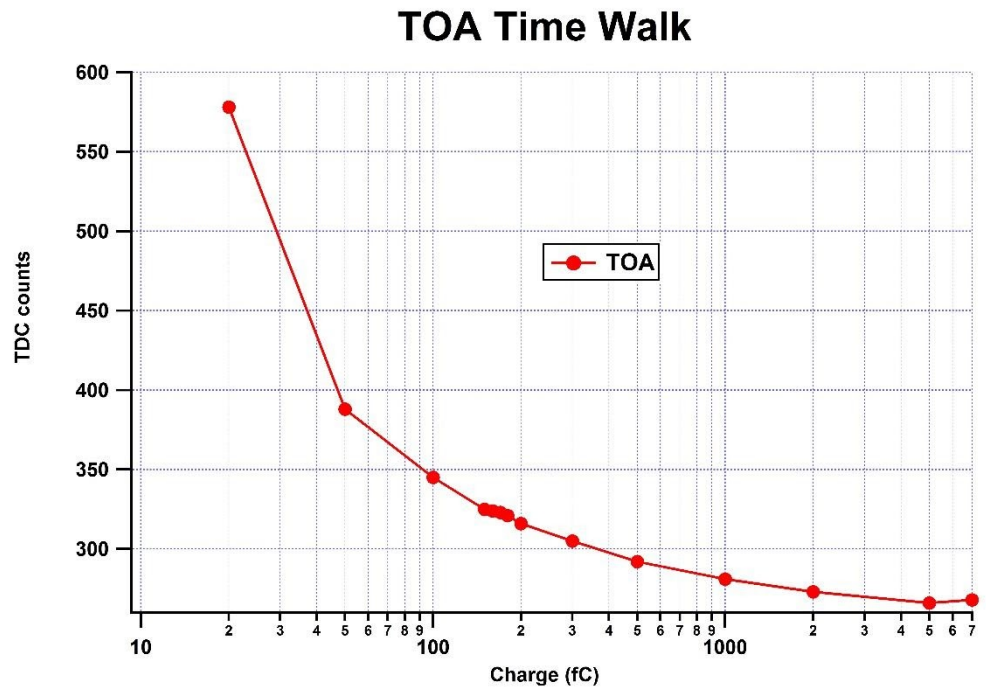


More detailed explanations about circuit, functionality and configuration can be found in dedicated documentation:

- **HGCROC_TOA_TOT_PLL_SPECIFICATIONS.pdf** describing the specifications of all parts designed by IRFU
  TO BE INCLUDED HERE

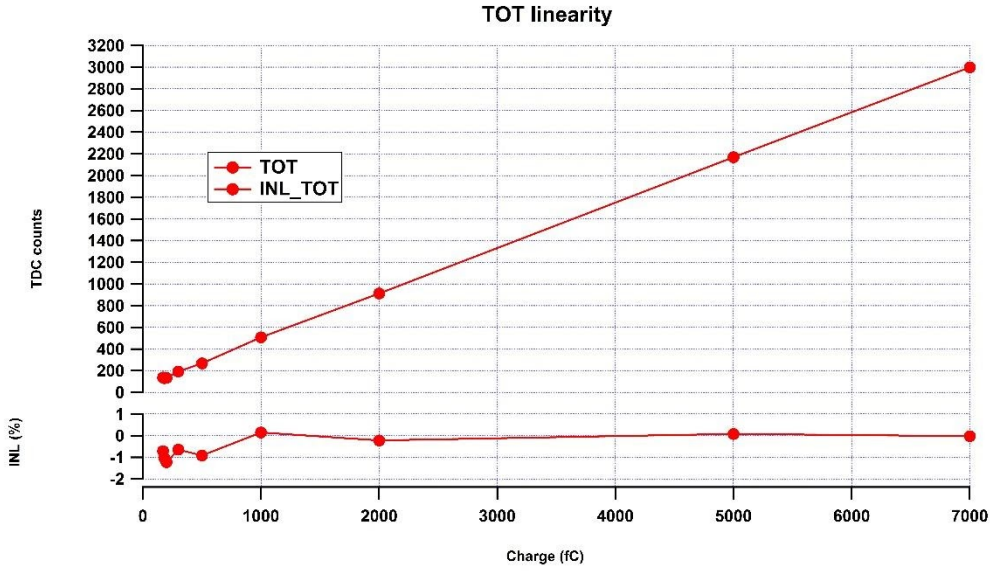
The following plot shows the digitized TOA time walk of HGCROC2.

325



326 The following plot shows the TOT linearity and the INL expressed in % of the dynamic range.

327



328

329 ## *1.2 1.3. Digital blocks*

330

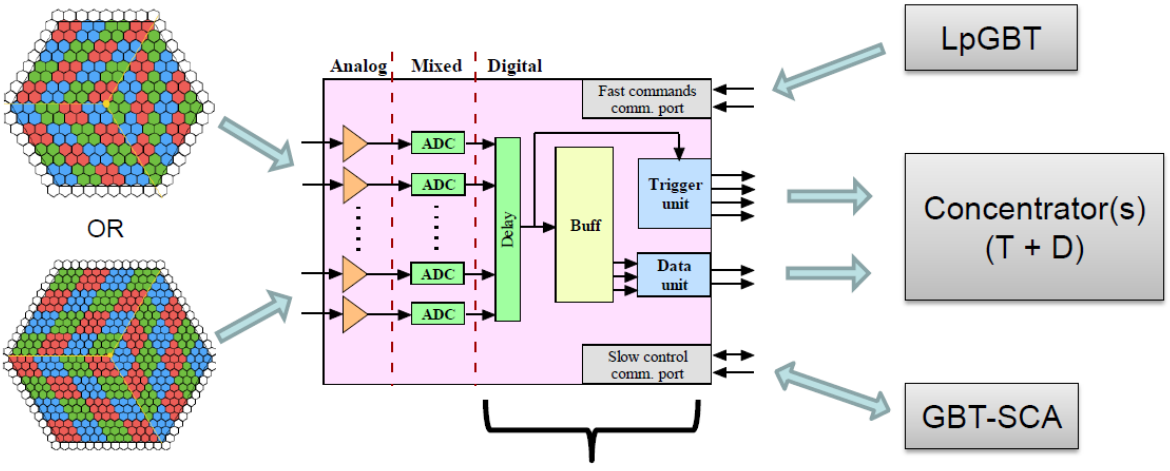
331 The main specifications of the digital part of the ASIC are described in the table below.

Analog channels	1. 72 analog "normal" channels 2. 4 for common mode channels 3. 2 for calibration
Acquisition mode	Continuous @ Bx rate (40 MHz)
L1 functionality	With derandomizer
L1-Trigger rate	1 MHz?
DAQ readout mode	• Triggered by L1A • … ?
Trigger data type	7-bit sums (4 or 9 channels)
DAQ data type	32 bits / channels (40 words/frame)
Trigger output port	4 x CLPS @ 1280 Mbps (2 used for 9ch sums)
DAQ output port	2 x CLPS @ 1280 MBps

HGCROC2 integrates 72 channels to readout

- 192 channels sensor with a 64-ch configuration
- 432 channels sensor with a 72-ch configuration

ADD RAM2 to this scheme



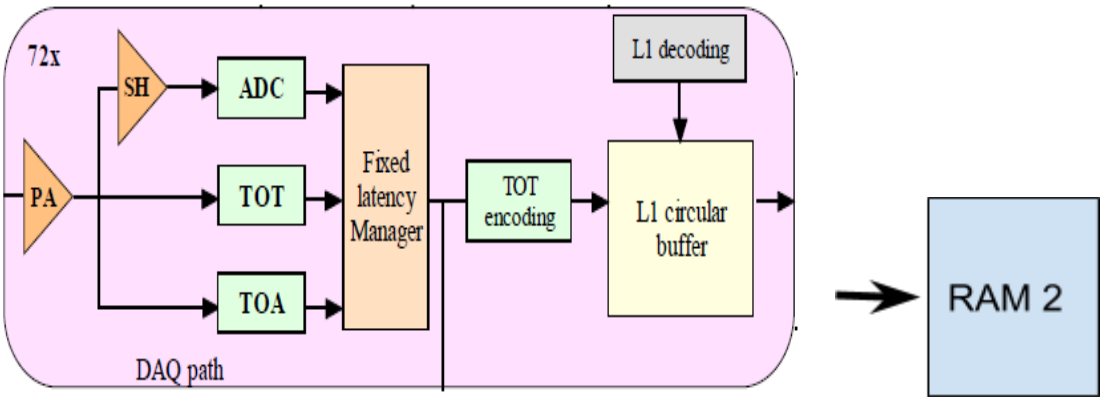
The document **HGROCv2_LinkSpecs_Guide.pdf** details the data path and the trigger path.
-> Incorporate details in this datasheet

1.3.1. Data path

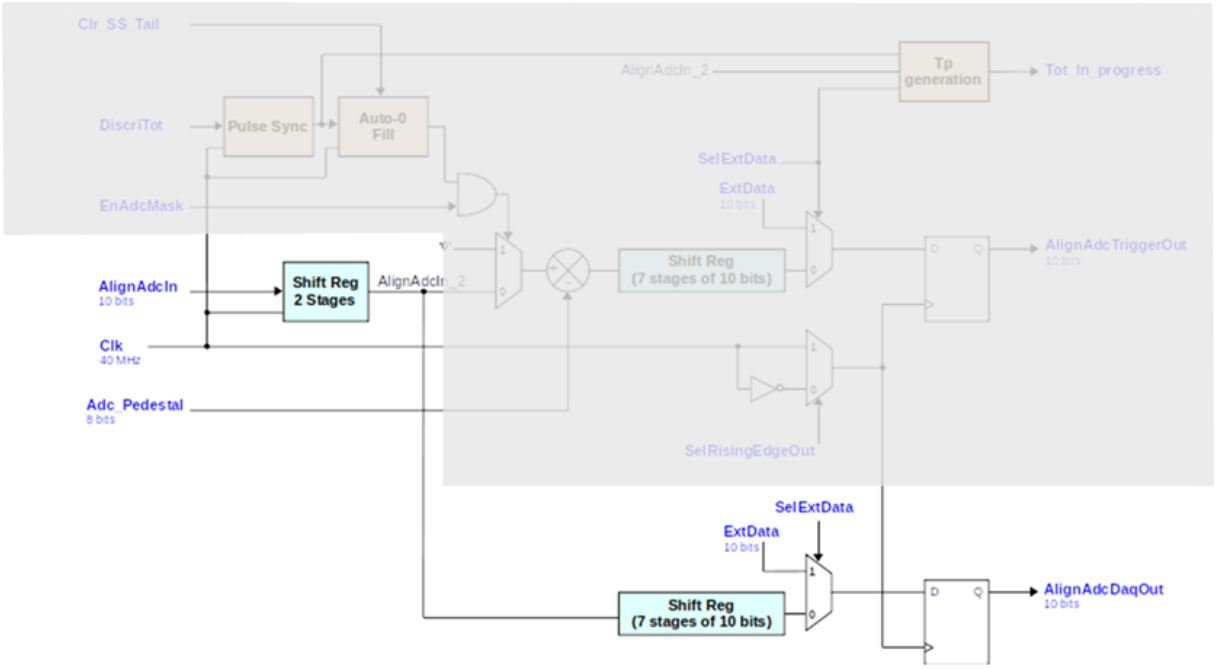
Following the Latency Manager block, the 3 pieces of channel information (ADC, TOT and TOA) are fed into the data path. The ADC values in the data path are without pedestal subtraction.
Common mode channels provide only the ADC data.

The figure below describes the functionality of the data path.

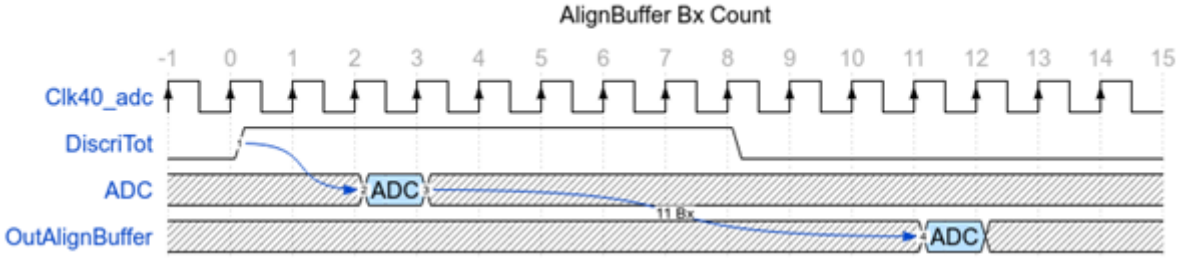
ADD RAM2 to this scheme



The figure below shows the AlignBuffer part of the DAQ path. By slow control, the user can force to send in RAM1 a programmed ADC value. Otherwise, the raw ADC data is always sent to the RAM1.



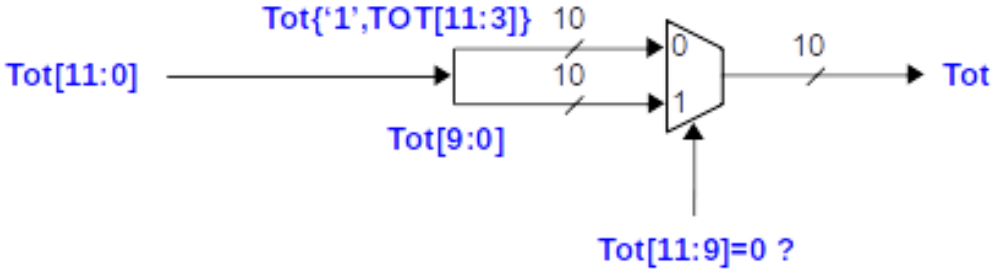
The figure below shows the chronogram of the AlignBuffer when EnAdcMask and Clr_SS_Tail = 0.



If EnAdcMask and Clr_SS_Tail = 1, we will have ADC = 0 for BXs from 0 to 11 (delayed of 11 BXs at the AlignBuffer output).

1.3.1.1. TOT compression

The TOT data are compressed from 12 bits to 10 bits. This operation is done in the digital block.



1.3.1.2. Data Path Content

The 30 bits of the Data Path content is shown in table Table 1.

	ADC (t-1)	ADC (t)	TOT	TOA	Charge collection	Data type
1	x	x		x (=0)	Q < TOA_thr AN	Normal
2	x	x		x	Q < TOT_thr AN	Normal
3	x		x	x	Q > TOT_thr AN	Normal
4		x	x	x		"Characterization"

Table 1: The Data Content

The old confused "calibration mode" is renamed "characterization mode", it is set by slow control. The specificity of this mode is to have ADC, TOA, TOT of the same event and TOT in 12 bits. It is dedicated for characterization and debugging.

Two flags are added to the 30 bits in order to remove some ambiguities which can occurs in the data path:

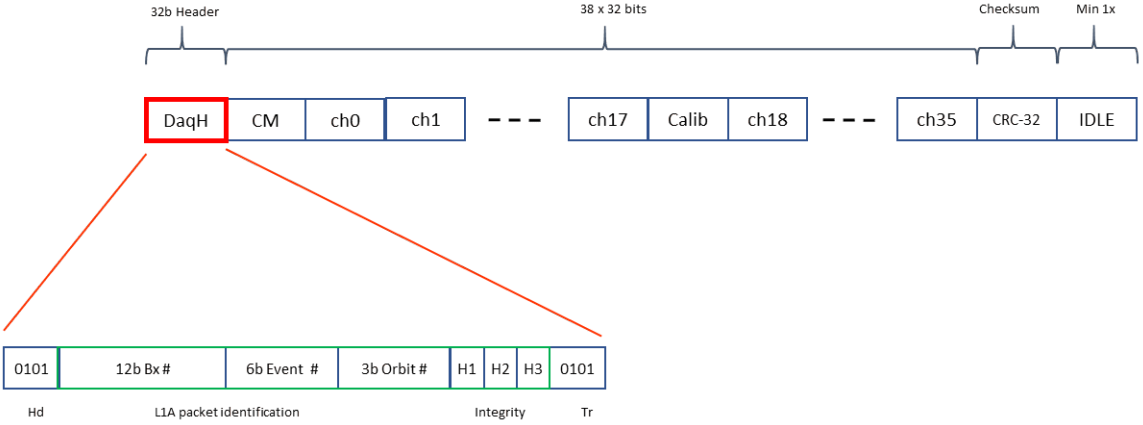
1. TOT-In-Progress, Tp, (applicable for lines 1 and 2 and 4 of the table): A TOT occurred in a previous BX and the ADC value can be "corrupted" (saturation or undershoot)
2. TOT-Complete, Tc, (applicable in lines 3 and 4 of the table): the second 10 bits packet corresponds to TOT, not ADC.

Note : The ADC values in the data path are without pedestal subtraction.

Tc and Tp Interpretation:

- 0b00 : The TOT is not in operation (not busy), normal behaviour with ADC data (TOT filled with 0)
- 0b01 : The TOT is busy (integration or undershoot), Tp highlights the fact that provided ADC correspond to saturation (during integration) or undershoot (TOT filled with 0)
- 0b10 : should not appear => we only output value when TOT is busy
- 0b11 : The TOT value is output, normal behaviour with TOT data (ADC value is between saturation and undershoot)

1.3.1.3. Frame Description



- Bx#: Value of BC on 12 bits.
- Event#: Value of EC on 6 bits, to detect if a L1 trigger was sent but related data wasn't saved (RAM2 full)
- Orbit#: Value of Orbit Counter OB on 3 bits.
- H1: Error during hamming decoding in Header.
- H2: Error during hamming decoding in CM to CH17 (1st Quarter).
- H3: Error during hamming decoding in Calib to CH35 (2nd Quarter).

The Calib channel's data content is the same than a normal channel.

The common mode channels' data content is as per below:

10	10b "00...00"	Adc CM0	Adc CM1

The packet integrity is checked by the CRC (Cyclic Redundancy Check) on 32 bits data width.
The polynomial to apply is 0x04C11DB7:

$$X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$$

One IDLE is attached at the end of the frame.

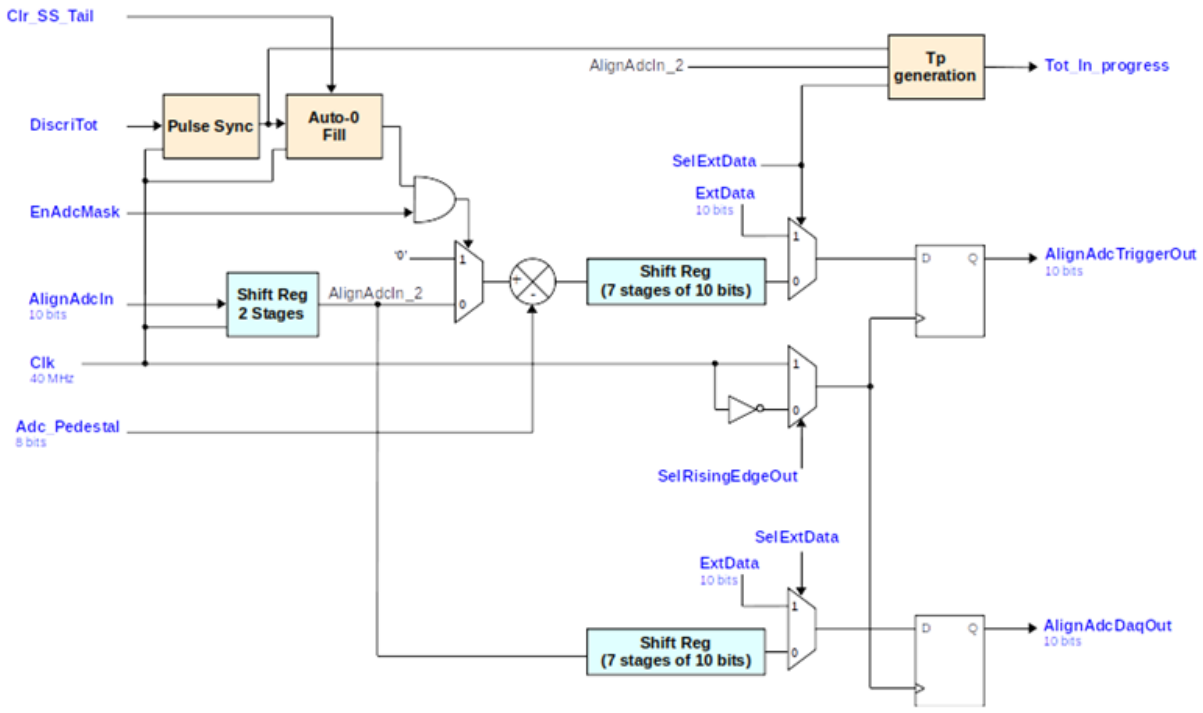
An idle packet is continuously sent out when no L1 trigger is activated. This Idle packet is configurable by slow control, the default idle word is CCCCCCC.

1.2.1 1.3.2. Trigger path

The data processing for the trigger path is composed as per below:

- Charge linearization over ADC/TOT range
- Sum of 4 or 9 channels depending on the sensor
- Charge compression to fit the bandwidth

The figure below shows the AlignBuffer scheme.
By slow control, the user can choose to force ADC to 0 when TOT pulse = 1 and/or three more BX (for the undershoot). Then the pedestal subtraction is achieved. By slow control, the user can force to send a programmed ADC value (global parameter).



1.3.2.1. Disabling channel

By slow control, ADC and TOT data can be forced to 0 per channel. This is made in the digital block after the AlignBuffer.

1.3.2.2. Trigger path content

Following the AlignBuffer block, the 2 pieces of channel information (ADC and TOT) are fed into the trigger path. There follows a Charge Linearization block and a summing block to create Trigger Sum cells.

1.3.2.3. Charge Linearization Block

The Charge linearization block treats the ADC and TOT charge in different ways. The two paths are shown below. It is a scheme of principle as actually the pedestal subtraction is made in the AlignBuffer.

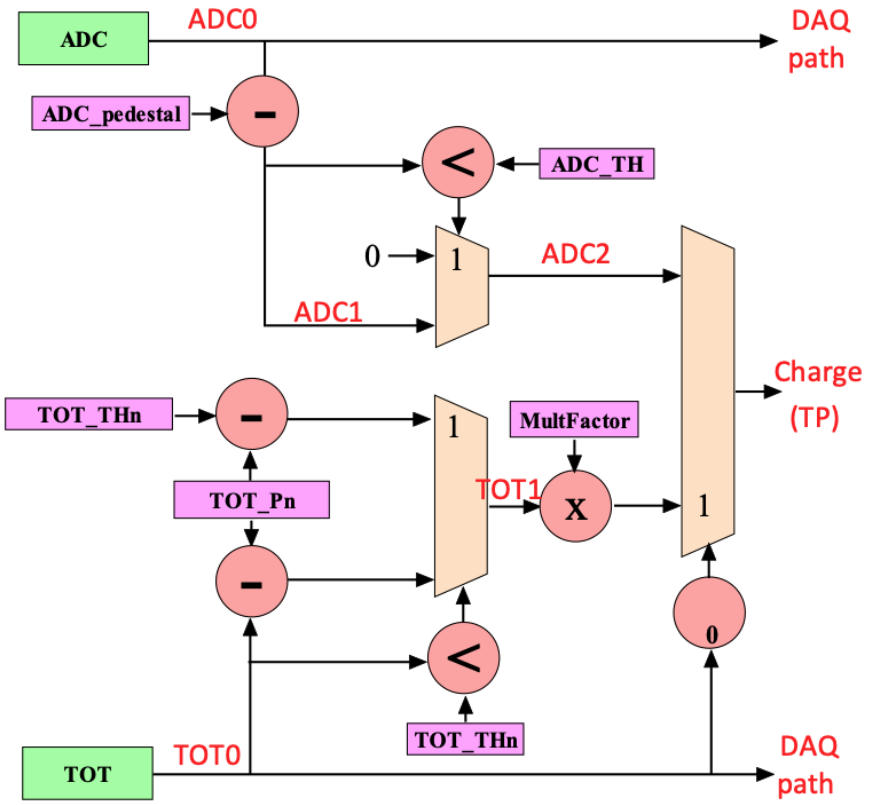


Figure: Charge Linearization Block

1.3.2.4. ADC Charge Processing

Referring to figure above, the ADC charge processing has 2 main steps

Step	Process name	Parameter	Action

1	Pedestal subtraction	ADC_pedestal (8 bits per channel)	If ADC0 > (ADC_pedestal + ADC_TH) then
			ADC2 = ADC0 - ADC_pedestal
			Else
			ADC2 = 0

2	Noise cancellation	ADC_TH (5 bits global per ROC)	

Note:

The constants are to be measured during a calibration phase and loaded via slow control. ADC_Pedestal is a dc offset per channel and ADC_TH is used for a noise cut.

1.3.2.5. TOT Charge Processing & Selection of ADC value or TOT.

The TOT charge processing and selection has 4 main steps.

Step	Process name	Parameter	Actions

1	TOT pedestal subtraction	TOT_Pn (7 bits per group of 9 channels)	If TOT0 > TOT_THn then
			TOT1 = TOT0 - TOT_Pn
			Else
			TOT1 = TOT_THn - TOT_Pn

2	Plateau or linear selection	TOT_THn (8 bits per group of 9 channels)	
3	Convert time to charge (ADC units)	Multifactor (5 bits global, default value = 25)	

4	Selection between ADC and TOT		If TOT0 ≠ 0 then
			Charge = TOT1 x Multfactor
			Else
			Charge = ADC2

Notes:

TOT_pedestal, TOT_threshold and Multiplication factor are parameters to be measured during a calibration phase and reloaded via slow control.
TOT0 is a 12 bit value obtained from the TOT block.
TOT pedestal, defines the TOT linear fit offset.
TOT threshold defines the lower limit of the TOT linear part
Multiplication factor = Ratio between the TOT and the ADC LSB

Finally there is the selection between charge from the ADC or TOT.

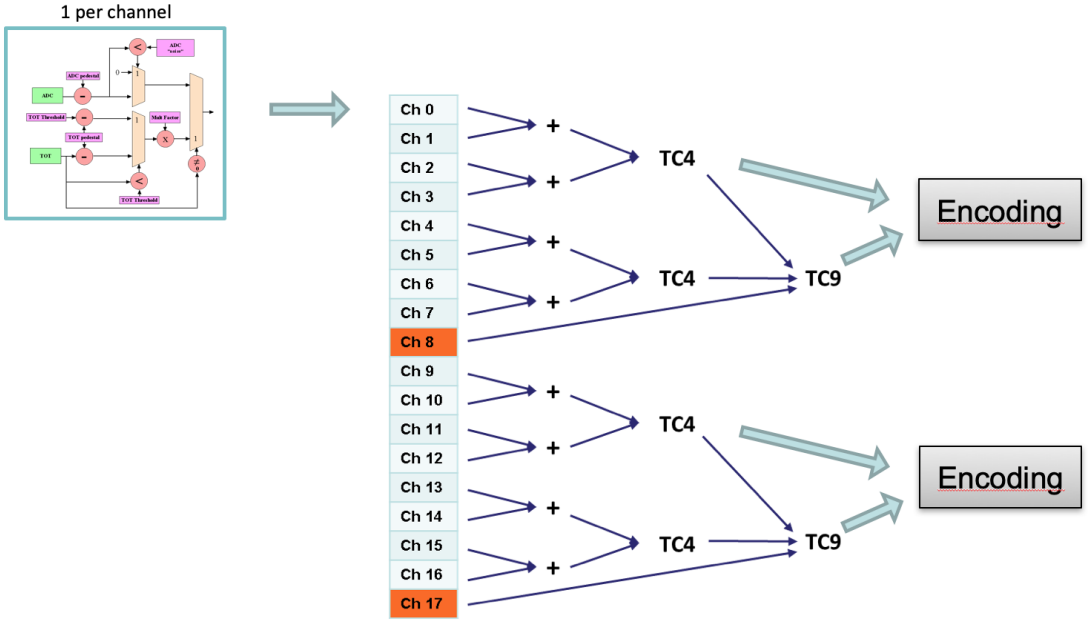
The value of the Multiplication factor allows to linearize the ADC range and the TOT range; it is coded over 5 bits in order to cope with the three typical gains:

- 31 for the 80fC ADC range
- 15.6 for the 160fC ADC range
- 7.8 for the 320fC ADC range

(The default slow control value is 25 for a theoretical 100fC ADC range.)

1.3.3. Trigger Cell Sums

The user can define the chip to sum charge in groups or 4 or 9 channels to obtain trigger sums.
The selection between the sum by 4 (TC4) or 9 (TC9) is done by the ASIC parameter “SelTC4”.



* "orange" channels only when sum of 9 channels

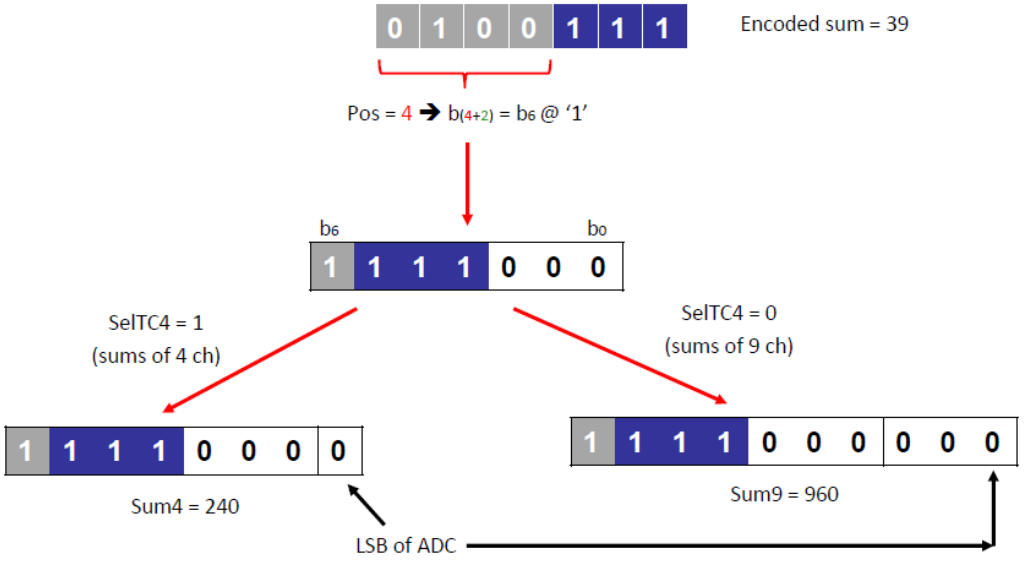
463 Figure 5: Channel Mapping for Trigger Sums

464 The sum by 4 gives 19b (12 TOT * 5b MultFactor) and sum by 9 gives 21 bits. We are using the encoding
465 over 7 bits with 4 bits for the position of the MSB + 3 bits to give the 3 next bits after the MSB, which
466 implies a maximum number of bit of 18. Consequently for the sum by 4, the LSB is removed; for the sum by
467 9, the three LSB are removed. We now have sum words over 18 bits and the encoding follows this logic:

468 - If Qin =< 7 ☐ Position = 0, bits = b2 b1 b0

469 - Else if Qin MSB @1 is bn ☐ Pos = n-2, bits = b[n-1:n-3]

470 And so the decoding can be described as per below.
471

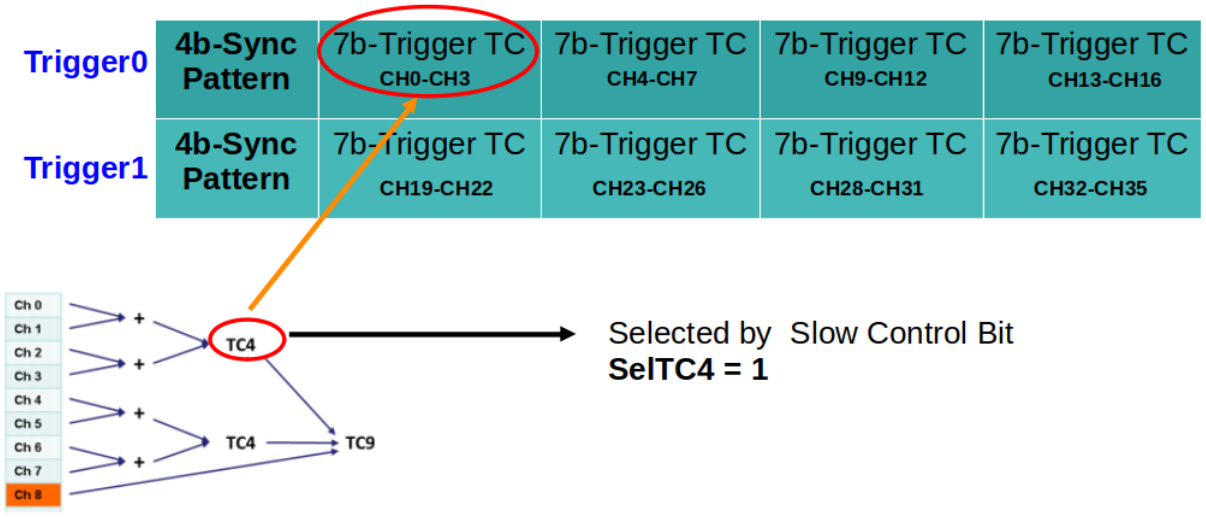


472

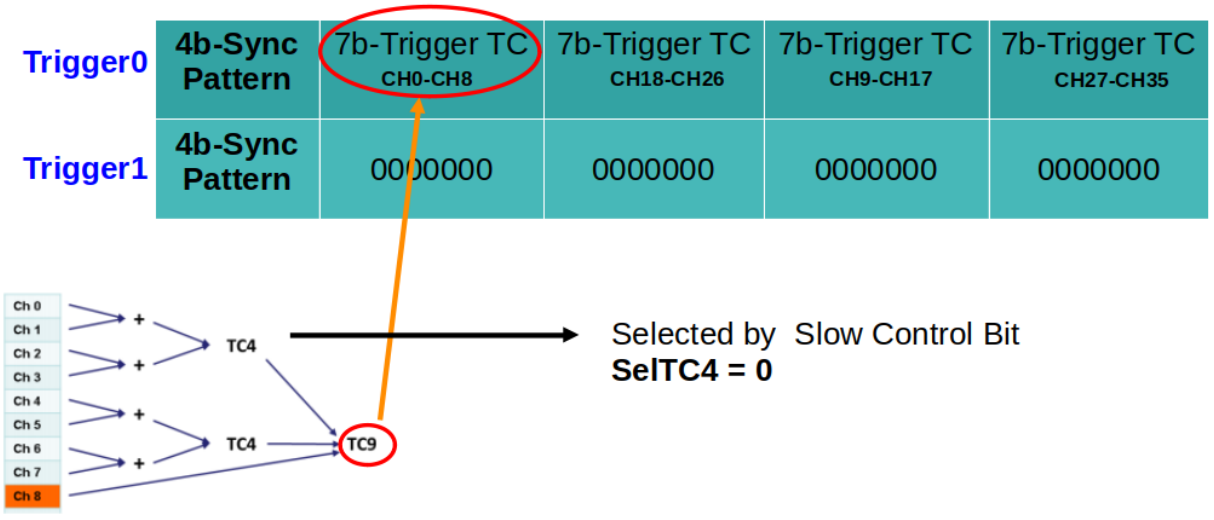
1.3.3.1. Frame description

The data transmission is MSB first.
The sum by 4 or 9 is set by slow control.
The Calibration and common mode channels are not in Trigger data.

The figure below shows the dataframe for the sum by 4.

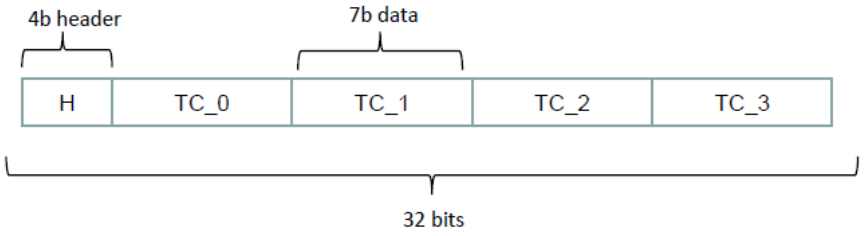


The figure below shows the dataframe for the sum by 9.



The table below gives an overview of the trigger path output format.

# Trig-link	4 or 2
Link type / speed	CLPS @ 1280 Mbps
Possible to switch-off unused link	Yes
# bits in 1 packet (each 25ns)	32
Packet composition (see below)	During startup: 1 header + 28-bit idle word else: 1 header + 4x Trigger Cell sums
Header	4 bits « 1010 » or « 1001 » @ Bx0
Trigger Cell mapping	See next slide
Trigger cell (TC) encoding	4b Exponent + 3b Mantissa
Bits order	MSB first



The content of the trigger data is depending on the SelTC4 setting.

Trig-link #0

H	TC0_0	TC0_1	TC0_2	TC0_3

	72 ch ASIC Sums of 9 ch	64 ch ASIC Sums of 4 ch
TC0_0	Sum ch ➔ 0 to 8	Sum ch ➔ 0 to 3
TC0_1	Sum ch ➔ 18 to 26	Sum ch ➔ 4 to 7
TC0_2	Sum ch ➔ 9 to 17	Sum ch ➔ 9 to 12
TC0_3	Sum ch ➔ 27 to 35	Sum ch ➔ 13 to 16

Trig-link #1

H	TC1_0	TC1_1	TC1_2	TC1_3

	72 ch ASIC Sums of 9 ch	64 ch ASIC Sums of 4 ch
TC1_0	0	Sum ch ➔ 19 to 22
TC1_1	0	Sum ch ➔ 23 to 26
TC1_2	0	Sum ch ➔ 28 to 31
TC1_3	0	Sum ch ➔ 32 to 35

Trig-link #2

H	TC2_0	TC2_1	TC2_2	TC2_3

	72 ch ASIC Sums of 9 ch	64 ch ASIC Sums of 4 ch
TC2_0	Sum ch ➔ 36 to 44	Sum ch ➔ 36 to 39
TC2_1	Sum ch ➔ 54 to 62	Sum ch ➔ 40 to 43
TC2_2	Sum ch ➔ 45 to 53	Sum ch ➔ 45 to 48
TC2_3	Sum ch ➔ 63 to 71	Sum ch ➔ 49 to 52

Trig-link #3

H	TC3_0	TC3_1	TC3_2	TC3_3

	72 ch ASIC Sums of 9 ch	64 ch ASIC Sums of 4 ch
TC3_0	0	Sum ch ➔ 55 to 58
TC3_1	0	Sum ch ➔ 59 to 62
TC3_2	0	Sum ch ➔ 64 to 67
TC3_3	0	Sum ch ➔ 68 to 71

H is always a 4-bit “1010” except at the first bunch crossing (BXCpt=0) where it is “1001”.

1.2.2 1.3.4. Digital parameters

The table below gives all the parameters of the digital block for the data and trigger paths, thus there are two of them in the chip as there are two digital blocks for the both sides of the chip.

name	# bits	comment
PllLocked	1	If available, status of PLL locked
CmdSelEdge	1	0: select fall edge for fast commands sampling (default)
SelTC4	1	1: sum by 4 / 0: sum by 9
SelRawData	1	1: send raw digitized data into RAM
IdleFrame	28	Default 28 LSB "1100---1100" of idle DAQ/T frame
L1Offset	9	L1 offset corresponding to L1 latency
Adc_TH	4	Threshold corresponding to noise in ADC count
MultFactor	5	TOT vs ADC ratio for linearization (default ~25)
Tot_P0,Tot_P1,Tot_P2,Tot_P3	7	TOT pedestal used in TP (common to 9 channels)
Tot_TH0,Tot_TH1,Tot_TH2,Tot_TH3	8	TOT threshold used in TP (common to 9 channels)

SelTCA, namely Select Trigger Cell of 4 channels, allows the user to select the sum mode: set to 1 to sum 4 channels, otherwise sum by 9.

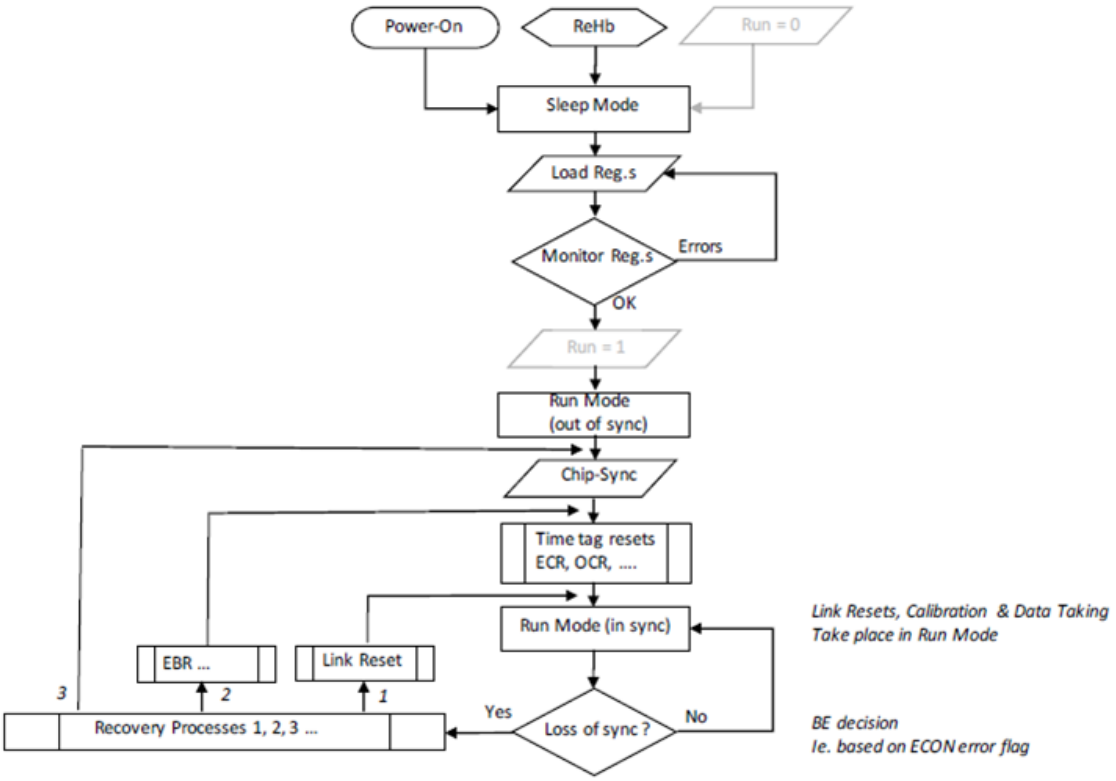
SelTC4		# channels used	# ch in each TC	# Daq-link @ 1,28G	# Trig-link @ 1,28G	unused channels
0		72	9	2	2	-
1 (default)		64	4	2	4	(8, 17, 18, 27) (44, 53, 54, 63)

1.2.3 1.3.5. Description of the operating modes of the chip

The hard reset pin ReHb (CMOS input, active low) reset all the chip: PLL, FastCommand block, I2C block, all the FSM, all the counters, all the D-FlipFlops, but not the slow-control parameters.
The hard reset pin ReSb (CMOS input, active low) reset only the slow-control parameters to their default values.

1.1 1.3.5.1. Start-up sequence

This section describes the start-up sequence of HGCROC-v3 chip.



When the chip is powering on, the Power-On-Reset (POR) block applies a reset (ReHb). The POR block can be disabled by a pin (Power-On disable).
By default, the slow-control parameter RUN is set to 0.

- RUN = 0 → SLEEP mode, StartUp_Ok = 0
  - FastCommand, I2C, PLL, SerDes ON
  - Low Power mode ON
  - IDLE pattern in Trigger and DAQ paths
  - RAM1 writing disabled
- RUN = 1 → RUN mode, StartUp_Ok = 1
  - FastCommand, I2C, PLL, SerDes ON
  - Low Power mode OFF
  - DAQ and Trigger paths: normal operation mode
  - RAM1 writing enabled

Low Power mode disables the analog part of the chip: preamplifier, shaper, discriminators. But since the PLL is ON, the ADC, TDC, AlignBuffer will be ON.

We will need to be able to synchronously reset some blocks (e.g. the TDC) when the chip enters in RUN mode. For now, we don't know exactly how to implement this.

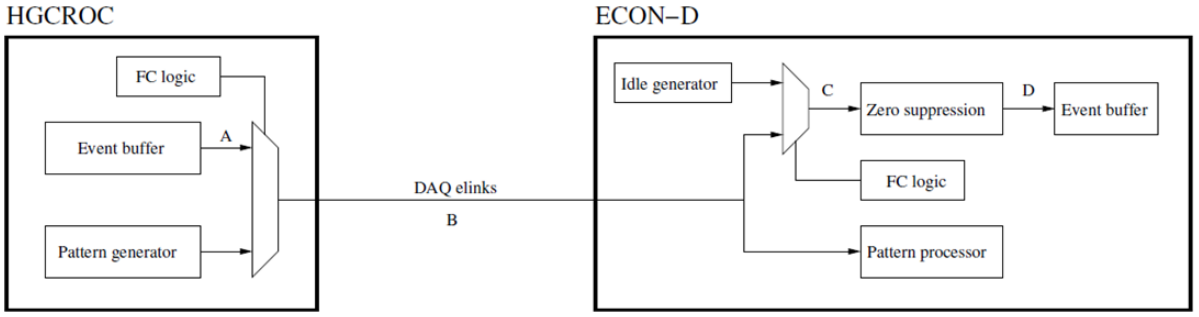
1.2 1.3.5.2. RAM1 to RAM2 operation

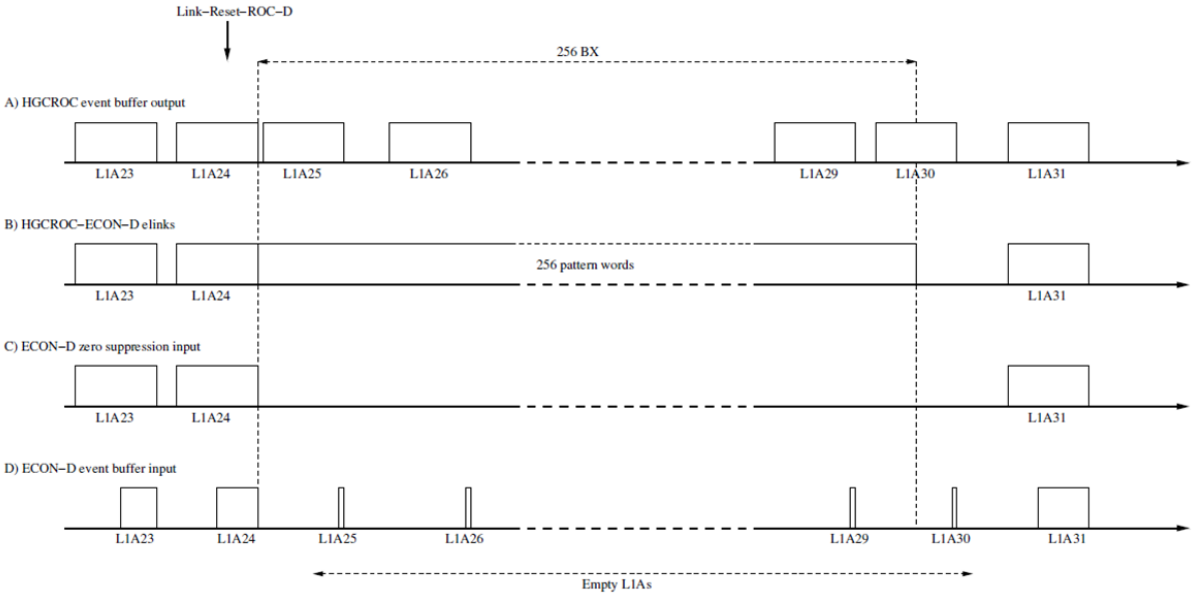
This section describes the operations between RAM1 and RAM2.
When the chip receives a L1A, the data of the event which occured to the current BX minus the programmed L1 latency (typically 12.5 us or 500 BX) is written to the RAM2, EC is incremented.
To be able to handle consecutive L1A, a FIFO will be implemented which will store the address value (current BX - L1 latency).

- What is the time taken to read from RAM1 and write to RAM2 is requested in order to know how much the fifo length has to be
- Why store BC and OC in RAM1 and not in RAM2?

1.3 1.3.5.3. RAM2 to SerDes State-Machine

This section describes the read-out operations from RAM2 to the DAQ links.
As long as RAM2 is not empty, the chip sends out the data. If RAM2 is empty, the chip sends out the IDLE pattern.
As described in the two figures below, when the chip receives a Link-Reset-ROD-D fast command, it starts the link reset procedure but after the completion of the current data packet. During the link reset procedure, the RAM2 emptying is going on, its emptying is independent of the link resync.





2. 1.3.5.4. Definition of the Time Tag Counters

My comments are in red.

- Bunc Crossing counter (BC): [12b], Increment on bx (40MHz) Reset to offset on Chip-Sync, BCR Wrap to 1 if=3564 (plus special 4b header in trig path) [programmable offset, default = 0]. Need clarification, which one of the two following statements is correct?
  - When the chip receives BCR or Chip-Sync, BC is set to programmed value AND special header (0x9) is added to the trigger path at current BX + programmed delay (delay on 12 bits)

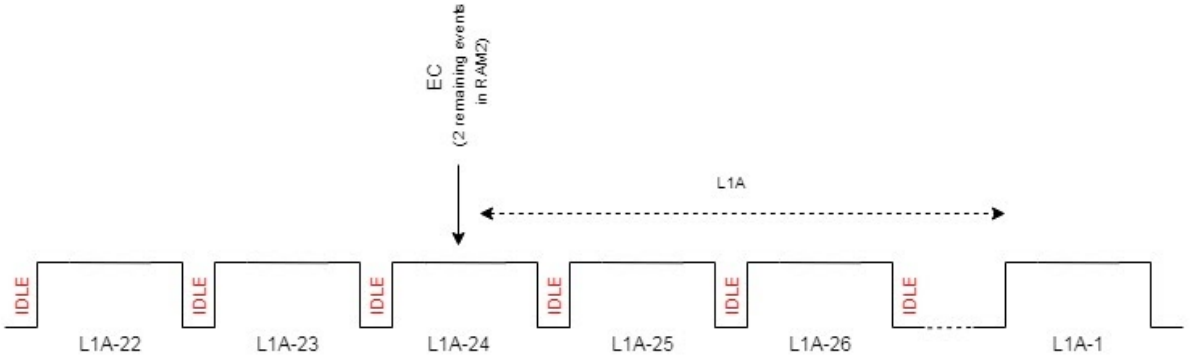
- When the chip receives BCR or Chip-Sync, at current BX + programmed value, BC is set to programmed value AND special header is added to the trigger path

- Event Counter (EC): [6b], Increment on L1A, Reset (EC=1) on ECR & ChipSync (first event after ReSync is EC = 1)
  - The spec is that the next event after ECR or Chip-Sync has to be labelled EC = 1. Not necessary, reset EC to 1.
- Orbit Counter (OC): [3b] Increment on BC-Wrap, Reset on OCR+BCR and Chip-Sync to 0
  - OK

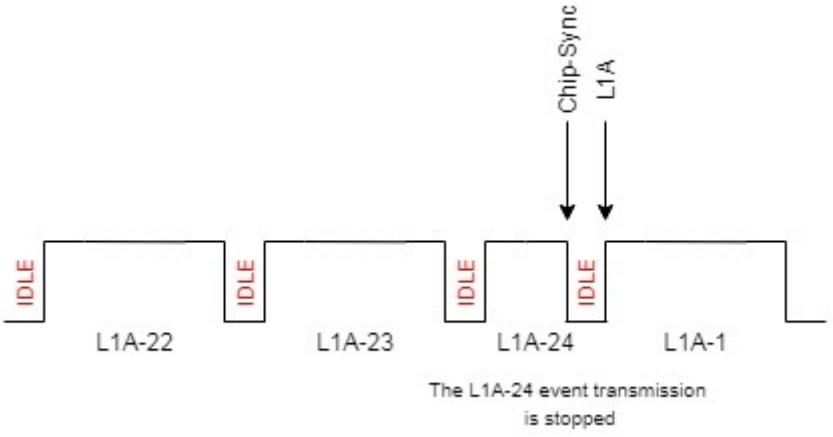
3. 1.3.5.5. Definition of the Reset

My comments are in red.

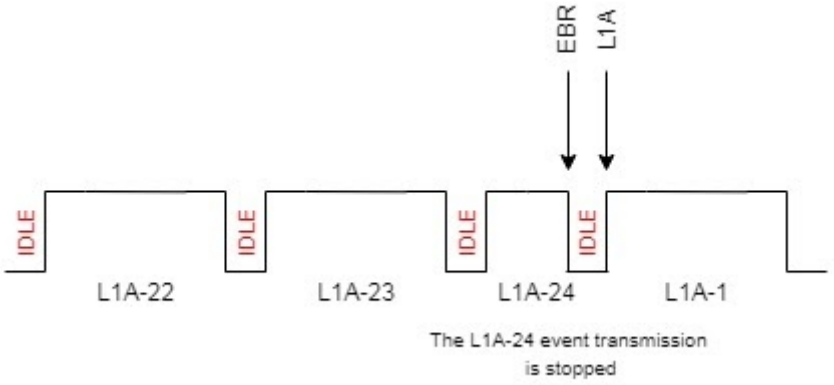
- Bunch Crossing counter reset (BCR): Fast Command, reset BC, see time tag table
- Event Counter reset (ECR): Fast Command, reset EC, see time tag table



- Orbit Counter reset (OCR): Fast Command, reset OC, see time tag table
- Chip-Sync: Fast Command, see time tag table, but also
  - data packets in RAM2 discarded?
  - write address of RAM1 reset to 0?
  - reset TDC counter?
  - ROC starts to send IDLE?
  - …



- Event Buffer Reset (EBR): Fast Command, reset Event Buffer, ECR, but not OC and BC. Chip must be ready to accept L1A in the next BX. Chip starts to send IDLE.



- ReHb: Resets every to default values and all SM to S0. Reset PLL in ROC.
  - Resets the FastCommand blocks, I2C block (not slow control parameters), ADC, TDC, digital block
- ReSb: Same ReHb but leaves the SC parameters programmed.
  - Resets only SC parameters, it seems to me safer to have two separate "reset domains", without "overlapp" (which implies a OR in the reset path).

1.4. Interfaces blocks

1.4.1. Fast command

The Fast Command stream is used to derive the 40 MHz master clock for the HGCROC.

See
https://indico.cern.ch/event/882853/contributions/3722675/attachments/1979350/3295476/Fast_Commands_Jan20.pdf

- Timing diagram of each Fast Command is requested.

Some details:

- CalPulseInt: send STROBE pulse to the internal calibration DAC. The STROBE pulse length is programmable (6 or 7 bits counter at 320MHz). The STROBE pulse phase can be adjusted within 25ns at 1.56ns step.
- CalPulseExt: send STROBE pulse to the external pin SiPM_calibration. The STROBE pulse length is programmable (6 or 7 bits counter at 320MHz). The STROBE pulse phase can be adjusted within 25ns at 1.56ns step.

The length and the phase of the STROBE pulse are set by slow-control.
Sending Fast Command CalPulse{Int/Ext} does not change the data content mode.

1.4.2. I2C

The document **HGCROCv2_configure_command_Guide.pdf** details I2C. Include missing info here.

I2C protocol is used to access ASIC parameters. Main features are given in the table below:

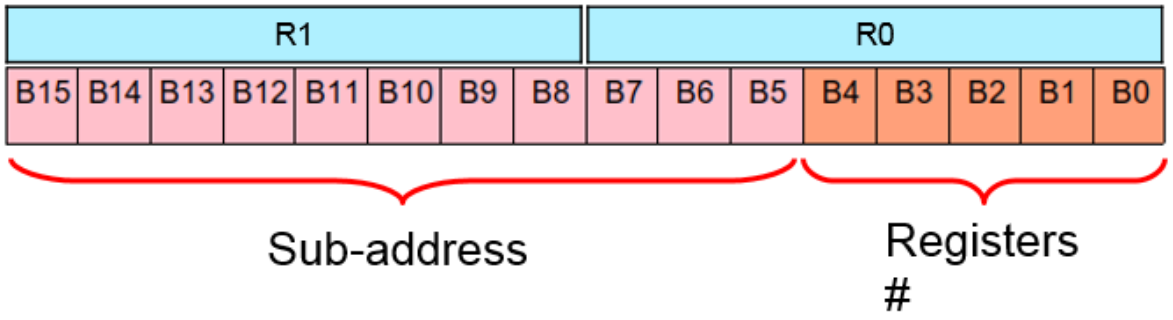
I2C	Detail	Comments
Chip addressing	4 bits	MSB of I2C first byte
Direct-access register addressing	3 bits	Register R0 to R7
"Burst" writing / reading	Yes	Accessible through R3
I2C speed	1M (max)	To be measured on HGCROCDv2
TMR	Yes	

The I2C circuits of the chip has 8 internal registers whose the use is described in the table below:

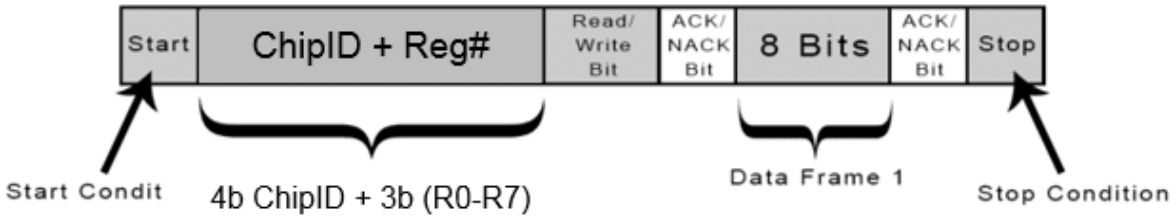
I2C @	Register	Comments
R0	ASIC parameter address (LSB)	Indirect @
R1	ASIC parameter address (MSB)	Indirect @
R2	Data	
R3	Data with auto @++	Increment indirect @ after each access
R4-R5-R6	Direct access SC-register	
R7	Status register (error, parity)	Read-only

To cope with the large number of parameters, extended addressing is used:

- 512 sub_address can be addressed (B15, B14 not used and have to be set to 0)
- Each sub_address has max 32 configuration parameters
- Extended addressing realized through 2 direct access registers: R0 and R1

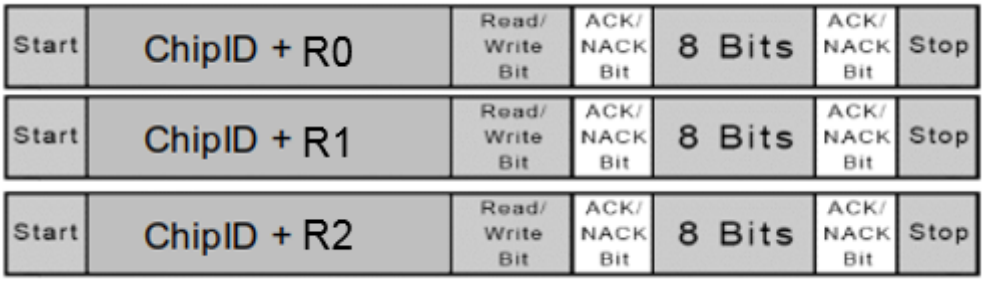


The frame of the I2C protocol is always the same:

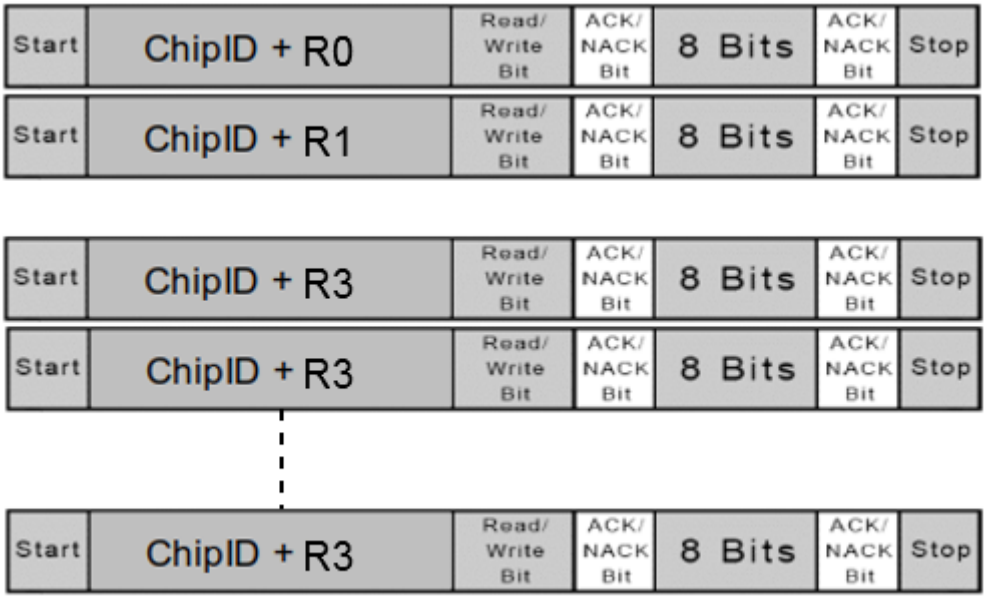


To write, set R/W bit to 0 and to read set R/W to 1.

For instance, to set a specific 8b word of the chip, the users has to write into the R0 register then R1 register to select the good parameters register address, and then write the data into the R2 register.



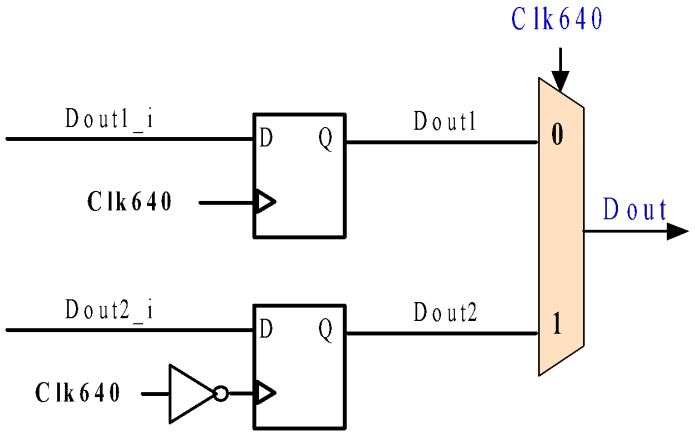
The user can also write into consecutive parameters register addresses: rather to write the parameters into the R2 register, he has to write successively into the R3 register.



1.4.3. Output E-links

The output differential links are composed of a serializer and a driver compatible with the LpGBT protocol (CLPS). The serializer converts parallel 32 bits words at 40 MHz to a serial train of bits send out at 1280 MHz.

New serializers without ReSyncLoad wrt HGCROCv2. ReSyncLoad will be removed and the SerDes will be autonomous. The internal logics will be partially triplicated.



In the table below, the electrical specifications of the driver are given.

Specification description	Value
Vcm (common voltage)	0,6 V
Vdiff (differential voltage)	100 to 200 mV
Pre-emphasis current	0,5 to 4 mA
Termination load	100 Ω

The termination load resistor must be placed outside the chip.

The register 5 of the "TOP" I2C sub-address allows to configure the current and the pre-emphasis of the driver.

Bit	Name	Default	Description
0	EN1	"1"	Current value of the CLPS drivers (Data/Trigger)
1	EN2	"1"	
2	EN3	"0"	
3	EN-pE0	"0"	Current value of the CLPS pre-emphasis driver (Data/Trigger)
4	EN-pE1	"0"	
5	EN-pE2	"0"	

6	S0	"0"	Delay value of the CLPS pre-emphasis driver (Data/Trigger)
7	S1	"0"	

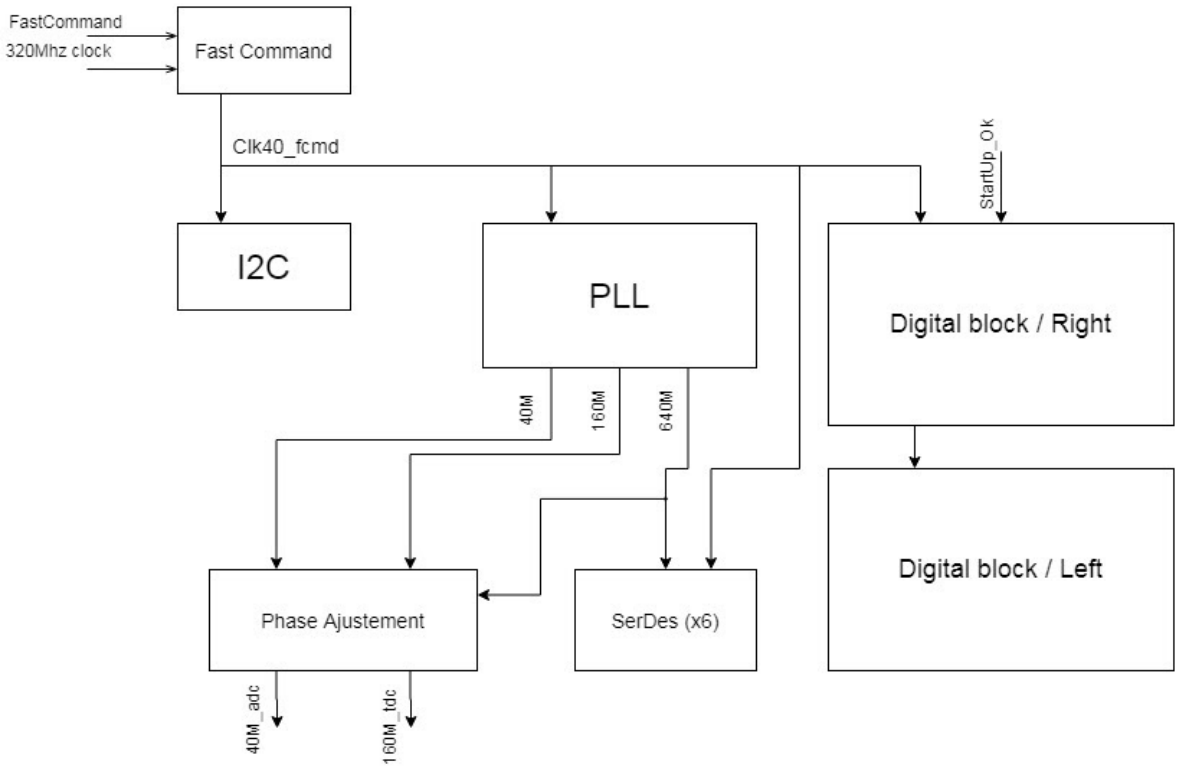
1.5. Ancillary blocks

1.5.1. PLL and clocks distribution

The main specifications of the PLL are described in the following table:

PLL specifications	
Input frequency	40 MHz (LHC bunch clock)
Output frequencies	1.28 GHz and 640, 320, 160 MHz
Jitter cleaner	Low jitter < 15 ps RMS (for an input jitter of 30 ps RMS)
Power consumption	< 2 mW
Area	Pitch 200 µm
Technology	TSMC 130 nm
Temperature	-30 °C

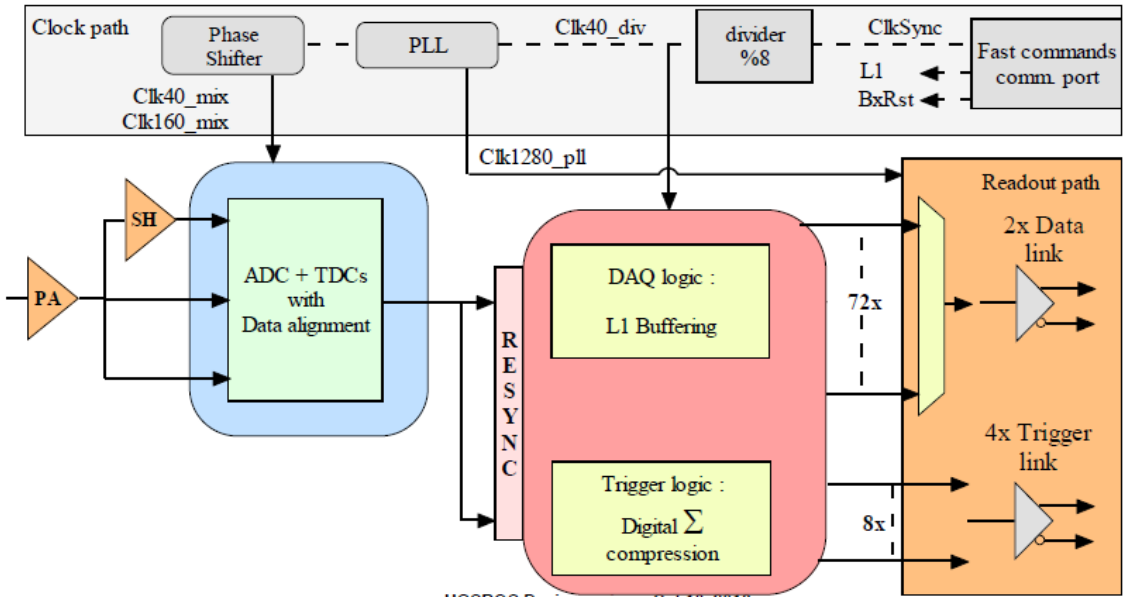
The chip only receives the Fast-Command link made of the 320 MHz fast command and the 320 MHz clock. The FastCommand block decodes the fast command and the 40 MHz clock in phase with the LHC. This 40 MHz clock is used for the I2C block, all the FSMs, the counters, the two RAMs, the wr/rd pointers and is the PLL reference clock. Only the hard reset ReHb allows to stop or re-start this clock by resetting the FastCommand block.



The PLL takes as reference clock the 40 MHz clock provided by the FastCommand block. The PLL can only be reset by the hard reset ReHb. The PLL generates three clocks: clk_40M_pll, clk_160M_pll, clk_640M_pll.

- Clk_40M_pll: this clock comes in a Phase Shift block to achieve the ADCs clock
- Clk_160M_pll: this clock comes in a Phase Shift block to achieve the TDCs clock.
- Clk_640M_pll: this clock comes in the SerDes of the E-links.

The clock distribution is described in the figure below (HGCROCv2 diagram also valid for V3?)



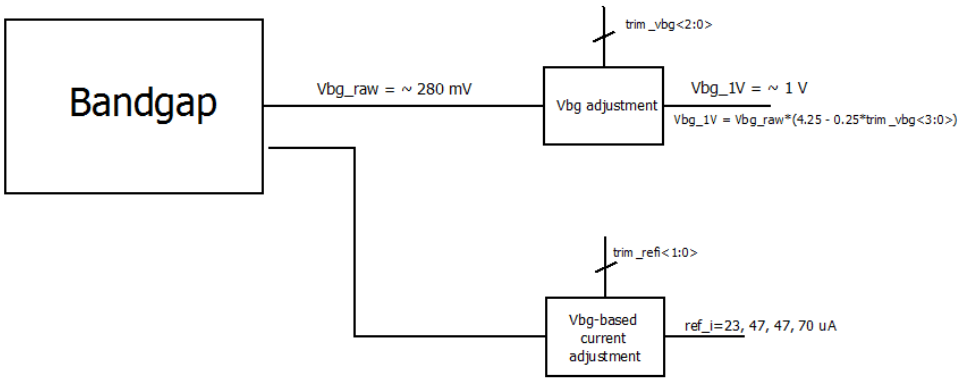
The shaper signal needs to be sampled to its maximum in order to optimize the signal-to-noise ratio; to do that the phase of the 40MHz sampling clock needs to be adjustable. The phase is adjusted by steps of ~ 1.5 ns (640 MHz period).

Some parameters, described in the “TOP” sub-address section, allow to configure the PLL.

1.5.2. Bandgap and voltage references

See the document **datasheet_BGP_130nm.pdf** for detailed information about the bandgap.

Typically, the bandgap provides an output voltage of around 280 mV. We need to multiply this value to get a usable voltage reference around 1 V. From the bandgap voltage, a Vbg-based current is provided as well.



The Vbg_1V is used to generate the upper reference voltage of the Calibration 11b-DAC, the reference voltage of the ADCs, ref. voltage for the TDCs, bias and to keep the TOT insensitive to the power supply variations. The ref_i reference current is used to generate the offset and the steps of the 10b-DACs.

Four global 10 bits DACs provide voltage references for the analog part: the two discriminator thresholds, the inverted and non-inverted references for the shaper. As the circuit is symmetrical, there are two bandgaps and two sets of voltage references with DACs for the two right and left sub-parts.

The voltage references are fabricated from the bandgap (ref_i), the 10b DAC and the preamplifier output of a common mode channel (channels CM<1> and CM<3>) so that the chip is not sensitive to the temperature (see Design Review report for more detailed information).

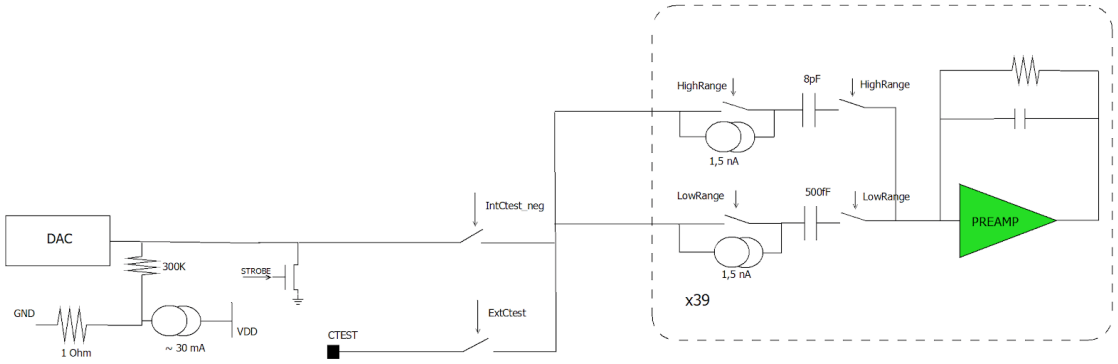
Note that since the reference voltages are made from the preamplifier output of CM<1> and CM<3>, these two channels are requested to be ON (the channel_off parameters cannot be set to 1 for instance for these channels).

1.5.3. Calibration circuit

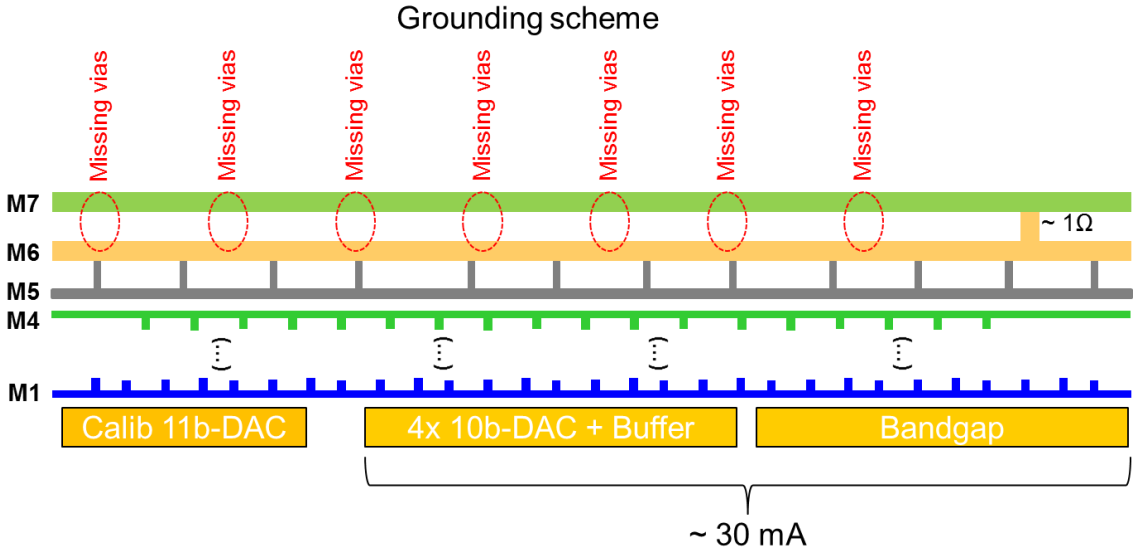
The following scheme shows the circuitry of the HGCROC-v3 calibration DAC. It is now a 12-bits DAC, the offset caused by the current flowing through the bandgap and the reference voltage buffers is removed by connecting the calibration DAC ground to the preamplifier grounding. Moreover, another source of offset is the gate leakage current of the switches (HighRange and LowRange) into each channels. Measurements on HGCROC-v2 show 7nA + 1.5nA*N_{CH_ON}, with N_{CH_ON} the number of enabled injection capacitances. This would introduce an offset of 1.2 fC for N = 1, 10fC for N=40, it is the reason why we also reduce the size of the LowRange switches (by a factor 5) in order to hopefully keep the offset lower than 1fC for N=1, 2fC for N=40.

Assuming the 12b-DAC provides a voltage up to around 1 V (the bandgap value), the user may set 0.5pF or/and 8pF injection capacitances in the chosen channels, to study the 0 – 0,5 pC range, the 0 – 8 pC range or, by setting the both capacitances, the 0 – 8,5 pC range. To correctly calibrate the ADC/TOT behavior, it is important to have an overlap between the available charge ranges.

The ctest node comes from an external pad and allows the user both to use an external pulser rather than the calibration DAC and also to calibrate the calibration 12b-DAC.



In HGCROC-v2, the 11-bit DAC had a ~30 mV offset when setting 0. The offset is relatively stable with temperature and irradiation. It was traced to a 1 Ω resistor in gnd_dac in which ~30 mA current is flowing to feed all the reference buffers. This resistance is lowered by M6-M7 connection and the calibration DAC is referred to gnd_pa rather than gnd_dac.
The following figure shows the HGCROC-V2 grounding scheme of the calibration DAC.



Finally, modifications to remove the calib_dac offset

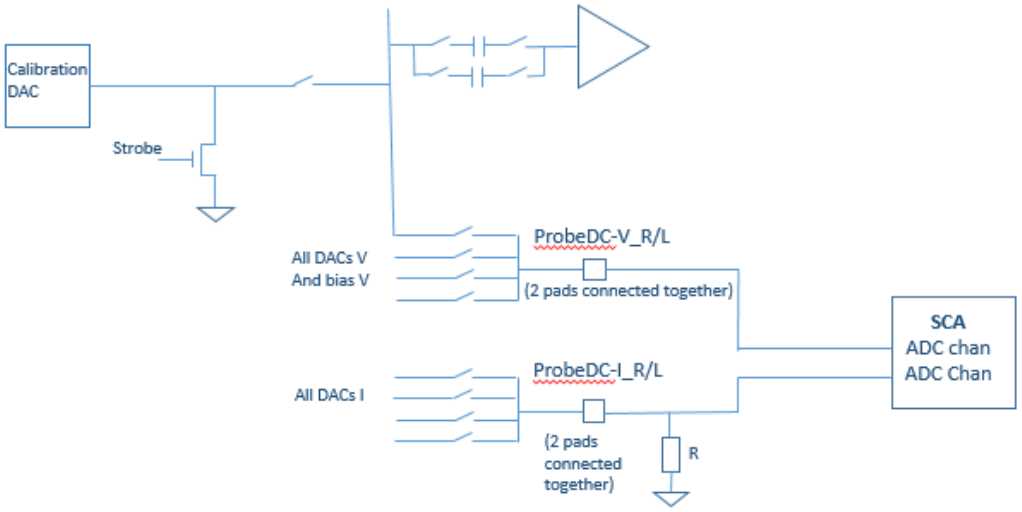
- The calibration DAC is 12-bit R2R instead of 11 bits.
- The ground is connected to gnd_pa instead of gnd_dac.
- The strobe switch is connected to gnd_pa instead of vss.
- The output switch is removed to reduce gate leakage.
- The switch to the in_ctest pad is reduced as it is used only for monitoring; Ctest goes now to the probe_DC_V through an analog multiplexer together with the others DACs.
- All the LowRange switches are reduced by a factor 5 to reduce the gate leakage and so the offset.

1.5.3.1. Strobe pulse length

The calib fast command lasts 1 clock cycle but the strobe pulse lasts more than 10-12 clock cycles to not inject the opposite charge in BX+1. A counter (6 or 7 bits at 320MHz) is implemented to achieve this. The phase of the strobe pulse w.r.t. 40MHz clock will be adjustable by delay of 1.56 ns (640 MHz).
A CalExt fast command sends a strobe to a pin.

A CalInt fast command sends a strobe to the internal CalibDAC.

1.5.4. Monitoring



The internal DACs outputs (calibration, reference voltages and Current DAC) will be multiplexed as described in the figure above. The signals will be sent to the ADC of the SCA chip.

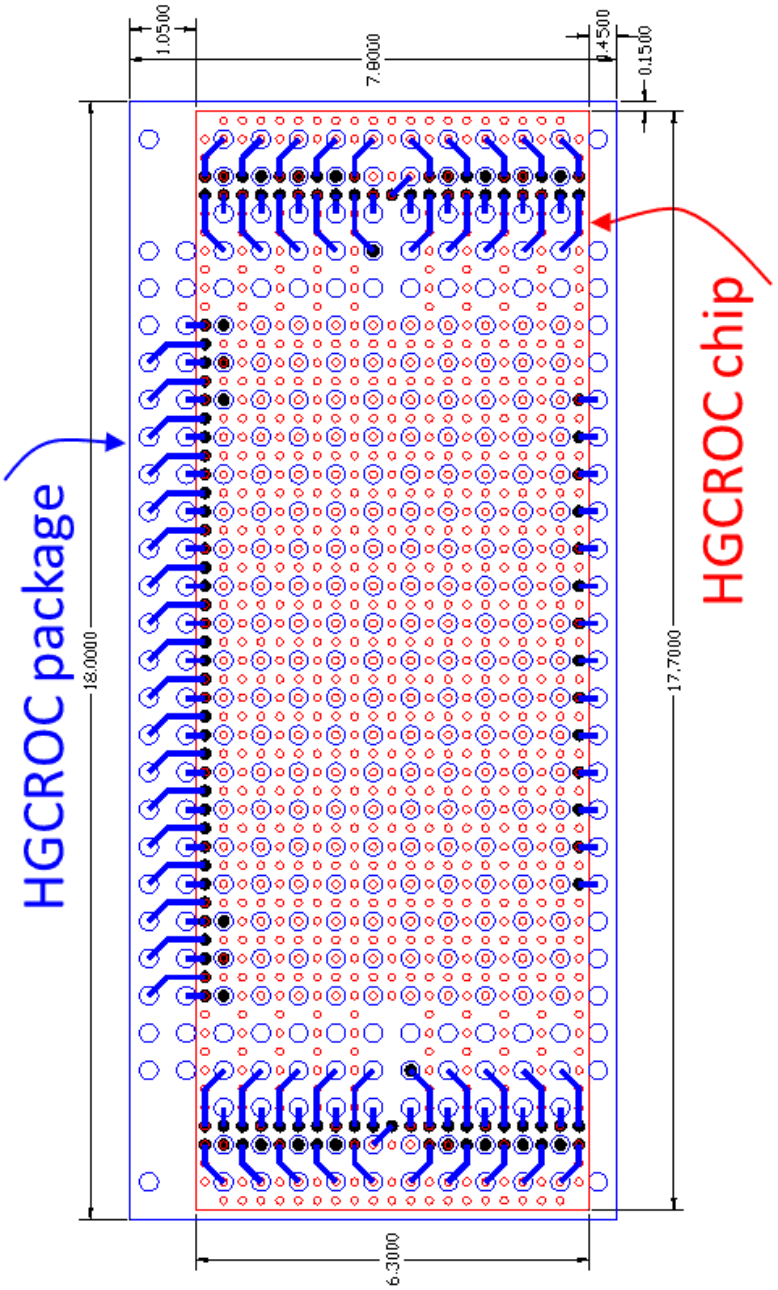
734

2. Packaging, I/Os and powering scheme

735 The chip pinout has been defined by the hexaboard constraints [Tommaso et al.] and the BGA package that
736 will be used to house the chips, as shown in figure below.

737

738



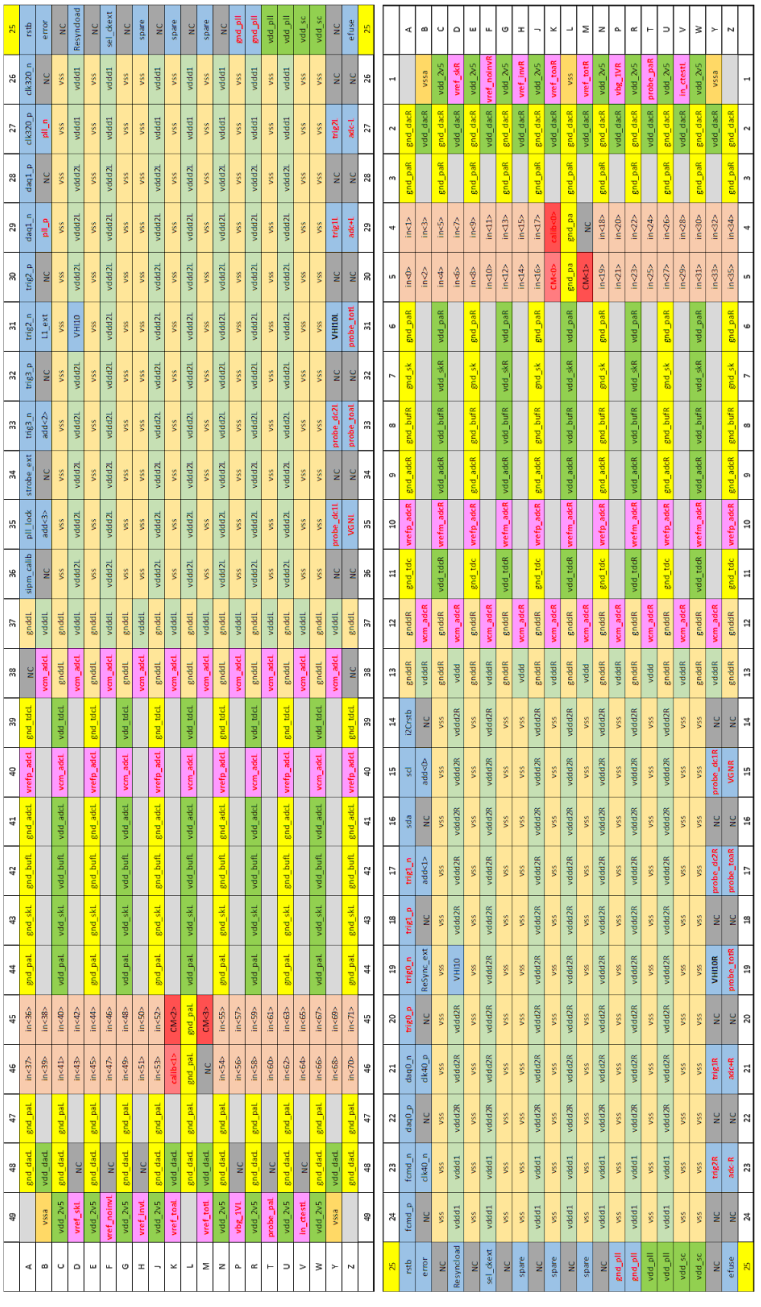
739

740 The two figures below show the left view and the right view of the die. Can be noticed the common column
741 25 in both figures.

742 TO BE UPDATE FOR ROC3

743

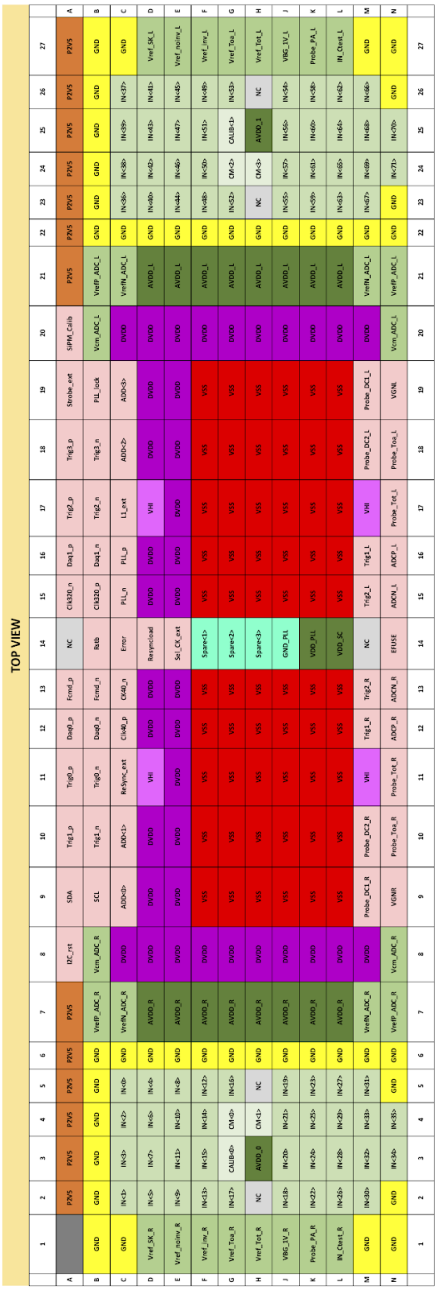
744



745

746 The figure below shows the top view of the BGA map as can be seen on the board.

747



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2.1. I/Os list

Names	Comment	Type	# ports	# signals	Level
Clk e-link	Fast commands @ 320M	Input	1	2	CLPS
FastCmd e-link	Fast commands @ 320M	Input	1	2	CLPS
Trigger e-link	Trigger @ 1,28G	Output	4	8	CLPS
DAQ e-link	DAQ @ 1,28G	Output	2	4	CLPS

I2C - SDA	I2C data	Bidir	1	1	CMOS
I2C - SCL	I2C clock	Input	1	1	CMOS
I2C - address	I2C address bonded on the board	Input	1	4	CMOS
Power-ON disable	Disable the POR	Input	1	1	CMOS
ReHb	Global reset, global to the hexaboard	Input	1	1	CMOS
ReSb	Slow Control reset	Input	1	1	CMOS
Error B **	Error Flag	Output	1	1	Open Drain
Efuse			1	1	
SiPM calibration***	Calibration enable (to strobe LEDs)	Output	1	1	CMOS
			Total	**28**	

(**) Error B. Error signal flagging a SEU event in the I2C register parameters. The implementation has to be defined.
(***) SiPM calibration. Only for the SiPM version of the chip.
The PLL locked signal will be accessible through a direct addressing I2C register.

Name	Comment	Type	# ports	# signals
Probe_DC_V	To monitor/calibrate vDACs, bias	Output	-	1
Probe_DC_I	To monitor/calibrate iDACs	Output	-	1
			Total	**2**

2.2. Pin List

	Pin Name	Pin type		Comments	Default value
POWERS/GRO	P2V5	POWER		analog pad ring power supply	1,2V
	AVDD_0	POWER		analog power supply	1,2V
	AVDD_1	POWER		analog power supply	1,2V
	GND	GROUND		analog ground	0V
	DVDD	POWER		digital power supply	1,2V
	VSS	GROUND		digital ground	0V
	VDD_PLL	POWER		PLL power supply	1,2V
	GND_PLL	GROUND		PLL ground	0V
	VDD_SC	POWER		Slow Control power supply	1,2V

UNDS					
	VHI_R	ANALOG		By default keep free ; for monitoring.	1V
	VHI_L	ANALOG		By default keep free ; for monitoring.	1V
Half part (ch. 36 to 71)	Vref_SK_R	ANALOG	Input/Output	Reference voltage of the Sallen-Key amplifier, value close to the preamp input voltage. By default must be kept free. Can be monitored/checked.	200mV
	Vref_noinv_R	ANALOG	Input/Output	Reference voltage of the non-inverted shaper. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	Vref_inv_R	ANALOG	Input/Output	Reference voltage of the inverted shaper. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	Vref_Toa_R	ANALOG	Input/Output	Reference voltage of the TOA threshold. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	Vref_Tot_R	ANALOG	Input/Output	Reference voltage of the TOT threshold. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	VBG_1V_R	ANALOG	Input/Output	BANDGAP voltage. Value can be tuned by slow-control. Default value = 1V	1V
	Probe_PA_R	ANALOG		preamplifier analog probe. Channel-wise	
	IN_Ctest_R	ANALOG	Input	By default, external pin test, but possibility to connect the calibration DAC output to this pin by slow-control.	
	VrefP_ADC_R	ANALOG	Input/Output	Positive reference voltage of the ADC.	
	VrefN_ADC_R	ANALOG	Input/Output	Negative reference voltage of the ADC.	
	Vcm_ADC_R	ANALOG	Input/Output	Common mode reference voltage of the ADC.	
	Probe_DC1_R	ANALOG	Input/Output	DC analog probe (bias, ref.)	

	Probe_DC2_R	ANALOG	Input/Output	DC analog probe (bias, ref.)	
	VGNR	ANALOG	Input/Output	VGN monitoring	
	Probe_Toa_R	CMOS	Output	TOA discri output probe. Channel-wise	
	Probe_Tot_R	CMOS	Output	TOT discri output probe. Channel-wise	
	Trig1_R	CMOS	Input	External trigger 1	
	Trig2_R	CMOS	Input	External trigger 2	
	ADCP_R	ANALOG	Input/Output	Analog non-inverted probe; positive ADC input	100mV
	ADCN_R	ANALOG	Input/Output	Analog inverted probe; negative ADC input	1,1V
	IN<35:0>	ANALOG	Channel input		200mV
	CALIB<0>	ANALOG	Channel input		200mV
	CM<1:0>	ANALOG	Channel input		200mV
Common pins	I2C_rstb	CMOS	Input	I2C reset; ACTIVE LOW	0V
	SDA	I2C signal		I2C data	
	SCL	I2C clk		I2C clock	
	Error	Open drain		Open collector; external resistor must be added. OR of all the slow-control cells' error signals	
	ADD<3:0>	I2C chip adress		I2C chip address	
	ReSync_ext	CMOS	Input	External ReSync selectable by Slow Control	
	L1_Ext	CMOS	Input	External L1 signal selectable by slow control	
	Strobe_Ext	CMOS	Input	External calibration signal selectable by slow control	
	SiPM_Calib	CMOS	Output	Calibration signal for SiPM	
	ReSyncLoad	CMOS	Input	Serializers synchronization signal	0V
	Sel_CK_ext	CMOS	Input	External 40MHz clock selection (debug purpose); ACTIVE HIGH.	0V
	Rstb	CMOS	Input	General reset; ACTIVE LOW	
	EFUSE	ANALOG		pin connected to an internal resistor. HGCROC2 => 100Ω. HGCROC2A => 1KΩ. H2GCROC2 => 10KΩ. H2GCROC2A => 100KΩ.	
	PLL_lock	CMOS	Output		
	Clk320_p	CLPS	Input	Fast command 320 MHz clock	
	Clk320_n	CLPS	Input		

	Fcmd_p	CLPS	Input	Fast command data	
	Fcmd_n	CLPS	Input		
	Clk40_p	CLPS	Input	40MHz clock for debug purpose	
	Clk40_n	CLPS	Input		
	PLL_p	CLPS	Output	PLL output probe	
	PLL_n	CLPS	Output		
	Daq0_p	CLPS	Output	Data 0 link	
	Daq0_n	CLPS	Output		
	Daq1_p	CLPS	Output	Data 1 link	
	Daq1_n	CLPS	Output		
	Trig0_p	CLPS	Output	Trigger 0 link	
	Trig0_n	CLPS	Output		
	Trig1_p	CLPS	Output	Trigger 1 link	
	Trig1_n	CLPS	Output		
	Trig2_p	CLPS	Output	Trigger 2 link	
	Trig2_n	CLPS	Output		
	Trig3_p	CLPS	Output	Trigger 3 link	
	Trig3_n	CLPS	Output		
	Spare<3:1>	NC			
Half part (ch. 0 to 35)	Vref_SK_L	ANALOG	Input/Output	Reference voltage of the Sallen-Key amplifier, value close to the preamp input voltage. By default must be kept free. Can be monitored/checked.	200mV
	Vref_noinv_L	ANALOG	Input/Output	Reference voltage of the non-inverted shaper. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	Vref_inv_L	ANALOG	Input/Output	Reference voltage of the inverted shaper. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	Vref_Toa_L	ANALOG	Input/Output	Reference voltage of the TOA threshold. Value given by an internal 10b_DAC. Can be checked/monitored externally. By default must be kept free.	
	Vref_Tot_L	ANALOG	Input/Output	Reference voltage of the TOT threshold. Value given by an internal 10b_DAC. Can be	

				checked/monitored externally. By default must be kept free.	
	VBG_1V_L	ANALOG	Input/Output	BANDGAP voltage. Value can be tuned by slow-control. Default value = 1V	1V
	Probe_PA_L	ANALOG		preamplifier analog probe. Channel-wise	
	IN_Ctest_L	ANALOG	Input	By default, external pin test, but possibility to connect the calibration DAC output to this pin by slow-control.	
	VrefP_ADC_L	ANALOG	Input/Output	Positive reference voltage of the ADC.	
	VrefN_ADC_L	ANALOG	Input/Output	Negative reference voltage of the ADC.	
	Vcm_ADC_L	ANALOG	Input/Output	Common mode reference voltage of the ADC.	
	Probe_DC1_L	ANALOG	Input/Output	DC analog probe (bias, ref.)	
	Probe_DC2_L	ANALOG	Input/Output	DC analog probe (bias, ref.)	
	VGNL	ANALOG	Input/Output	VGN monitoring	
	Probe_Toa_L	CMOS	Output	TOA discri output probe. Channel-wise	
	Probe_Tot_L	CMOS	Output	TOT discri output probe. Channel-wise	
	Trig1_L	CMOS	Input	External trigger 1	
	Trig2_L	CMOS	Input	External trigger 2	
	ADCP_L	ANALOG	Input/Output	Analog non-inverted probe; positive ADC input	100mV
	ADCN_L	ANALOG	Input/Output	Analog inverted probe; negative ADC input	1,1V
	IN<71:36>	ANALOG	Channel input		200mV
	CALIB<1>	ANALOG	Channel input		200mV
	CM<3:2>	ANALOG	Channel input		200mV

3. ASIC parameters

As described in section **1.4.2 I2C,** the I2C circuit has 8 internal registers; the four first are dedicated to write/read the slow-control parameters. Registers 4, 5 and 6 are direct access registers and the register 7 is a status register in read-only mode.

In the tables below, the content of the direct access registers is described.

Bit	Name	Default	Description
0	AutoReload	"0"	Allows to rewrite the value after a SEU
1	EdgeSel	"0"	Selection of the clock edge of the 320MHz clock
2	NA	"0"	
3	NA	"0"	
4	NA	"0"	
5	NA	"0"	
6	NA	"0"	
7	NA	"0"	

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I2C Register R5			
Bit	Name	Default	Description
0	NA	"0"	
1	NA	"0"	
2	NA	"0"	
3	NA	"0"	
4	NA	"0"	
5	NA	"0"	
6	NA	"0"	
7	NA	"0"	

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I2C Register R6			
Bit	Name	Default	Description
0	NA	"0"	
1	NA	"0"	
2	NA	"0"	
3	NA	"0"	
4	NA	"0"	
5	NA	"0"	
6	NA	"0"	
7	NA	"0"	

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I2C Register R7 (Status , read only)			
Bit	Name	Default	Description
0	Error		OR of all the slow-control cells' error signals
1	Parity		Parity of all the slow-control cells' values
2	Pll_Lock		Pll lock flag. "1" pll is locked
3	NA		
4	NA		
5	NA		
6	NA		
7	NA		

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3.1. I2C Addressing

770 The four first I2C registers, R0-3, allow to define the address and the data to write or read into the internal 8
771 bits registers distributed into the chip sub-parts. R0 and R1 define the address of internal 8 bits registers. R2

defines the data to write into the chosen internal 8 bits register. R3 allows the user to access successive register address.

The chip, from I2C protocol point of view, is divided in sub-blocks containing maximum 32 registers each. In consequence, the address in 16 bits (given in R0 and R1) is composed of two sub-address:

- The 11 MSB bits code the address of the sub-block
- The 5 LSB bits code the address of the register of the sub-block

The table below gives the address, the name and a short description of all the sub-blocks.

4. Measurements of v2 for inputs for HGCROCv3 specifications

4.1. Power consumption: RUN mode vs. SLEEP mode

For the SLEEP mode, Preamplifier, shapers, discriminators are switched off, StartUp_Ok = 0 (no writing in RAM1)
For the RUN mode, all the chip is ON.
The power consumption decreases by 60%.

4.2. Power consumption: HD vs. LD

For the LD hexaboard, we would like to turn off channels 8, 17, 26, 35, 44, 53, 62, 71.
If we use channel_off enabled (preamp input tied to ground) and ADC, TDC and AlignBuffer masked, the power consumption decreases by 3%.